A POWER QUALITY SOLUTION WITH LOW INVERTER RATINGS

BY

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In memory of my mother

&

To my wife Shwu-Yuann

and

my daughter Karen

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Abstract of Dissertation Presented to the Graduate School
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The feasibility of a three-phase current-fed inverter for active filtering of distribution system harmonics was investigated since most of the published works in this field have employed voltage-fed inverters.

The study showed that the voltage-fed hybrid filter generally has less conduction losses than the current-fed one no matter what types of passive filters are employed. From the loss standpoint, the current-fed inverter is suitable for the role of active filter only when it is in series with a parallel-resonant passive filter tuned at the fundamental frequency, instead of the popular compound series-resonant filters tuned at 5th, 7th, and 11th harmonics. The function of the parallel-resonant filter, inserted in between the point of common coupling and the output capacitor of the current-fed inverter, is to prevent high fundamental current from circulating in the inverter circuitry. The power (VA) ratings of the semiconductor components and power losses of the inverter therefore are reduced.

The study also revealed that, in contrast to the voltage-fed inverter-based hybrid filter, which requires both the load voltage and the line current to be sensed and functions correctly only under closed-loop feedback control, the current-fed inverter-based hybrid filter can perform active filtering simply by scaling the fundamental removed load current to be the duty ratio for the inverter.

Simulation works confirmed the analysis. With the duty-ratio directly derived from the load current, the current-fed inverter-based active filtering on a prototype one-branch distribution system loaded with a 3kW full-bridge diode rectifier has been done successfully. The results of the experiment are in accordance with the analysis. Using 3kW as the power base and selecting the semiconductor devices with appropriate ratings for the inverters, the inverter losses are 0.82% p.u. for the current-fed/parallel-resonant filter, 0.08% p.u. for the voltage-fed/parallel-resonant filter, and 2.09% p.u. for the current-fed/compound series-resonant filter with the same capacitance (150μF) in each passive filter. Increasing the capacitance increases the inverter losses in the conventional hybrid filter, but does not increase the inverter losses in the proposed configuration. However, the VA ratings of the parallel-resonant passive filter are twice the ratings of the series-resonant filter, and high inductances are required.

In summary, the proposed hybrid filter, consisting of a three-phase current-fed inverter and a parallel-resonant passive filter tuned at the fundamental frequency, is suitable for active filtering of distribution systems with low overall losses and low VA ratings of the inverter components. The control of this current-fed combination is simpler than the control of various voltage-fed combinations.

CHAPTER 1
INTRODUCTION

The advances in modern semiconductor devices development have increased the scope of applications for various electronic components and devices, such as in HVDC [1, Chapter 10], variable-speed motor drives [2], and various power AC-to-DC and DC-to-AC converters [3, 4]. With the increasing applicable ranges of voltage, current, and power, electronic components and devices have become the essentials in control, regulation, and power delivery of electrical power systems nowadays. With nonlinear V-I characteristics in nature, the growing application of power electronic devices increases the power demands and presents a serious power quality problem to power systems [5, 6, 7, 8, 9, 10, 11], especially in the distribution level [12, 13].

Nonlinear loads contribute to the quality deterioration of a power source through the generation of harmonic and fundamental frequency reactive currents. The load-generated harmonic currents interact with the finite distribution/transmission line impedance to produce harmonic voltages at every bus along the power system, which may cause serious hazards to the power system and other power users [1, Chapter 10]. The fundamental frequency reactive current wastes the generated power and may pose a stability problem [1, Chapters 2 and 11] to the control of power systems. The power quality can be further deteriorated if the sags and surges, caused by unbalanced three-phase currents, subsynchronous frequency currents, or large load transients, are presented in the supply voltage profile of the system.

Based on the requirement that, ideally, only in-phase voltages and currents of the fundamental frequency should exist in the power system, the quality of a power source can be categorized as

- corresponding total harmonic distortion (THD, expressed in % of the fundamental component) of load voltage and line current,
- power factor, PF, and
- % sag or surge of fundamental voltage of the power source.

The definitions of %THD, power factor, and sag/surge can be derived from Figure 1.1. From Figure 1.1(a), the %THD of line current i_s is defined as

$$\begin{aligned} \mathrm{THD_i} &= \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} \\ &= \sqrt{\sum_{h \neq 1} \left(\frac{I_{sh}}{I_{s1}}\right)^2} \\ \%\mathrm{THD_i} &= 100 \times \mathrm{THD_i} \end{aligned} \tag{1.1}$$

where i_{s1} is the fundamental component of i_s, and I_s and I_{s1} are the root-mean-square (rms) values of i_s and i_{s1}, respectively. The power factor (PF) of the power system with a nonlinear load is defined as

$$\begin{aligned} \mathrm{PF} &= \frac{V_s I_{s1}}{V_s I_s} \cos\phi \\ &= \frac{1}{\sqrt{1 + \mathrm{THD_i}^2}} \cos\phi \end{aligned} \tag{1.2}$$

where V_s is the rms value of line voltage v_s and ϕ is the phase angle between v_s and i_{s1} in Figure 1.1(a). From Equation (1.2), it is clear that the harmonic components of a nonlinear load current will yield a lower power factor, and hence make the power system less efficient, compared to a linear load with the same fundamental current and phase angle

between the voltage and current. Figure 1.1 and Equation (1.2) assume that the line voltage does not contain any harmonic component. If there are harmonics in the line voltage spectrum, Equation (1.2) is rewritten as

$$\begin{aligned} PF &= \frac{V_{s1} I_{s1}}{V_s I_s} \cos\phi_1 \\ &= \frac{1}{\sqrt{1 + THD_v^2} \cdot \sqrt{1 + THD_i^2}} \cos\phi_1 \end{aligned} \tag{1.3}$$

where V_{s1} is the fundamental rms value of v_s; ϕ_1 is the phase angle between the fundamental voltage and current; and THD_v is the total harmonic distortion of v_s. When the load is nonlinear, the current harmonics are always accompanied by the voltage harmonics and the efficiency of the power system is further reduced.

All major industrial standards impose power quality guidelines on electrical utilities, users, and electrical equipment manufacturers in order to maintain an acceptable power quality for all parties [14]. For power utilities and users, the responsibilities can be simply classified as follows:

- to suppress the %THD of voltage supplied to users and
- to stabilize the fundamental frequency voltage

for the power utilities, and

- to suppress the %THD of current injected into utilities and
- to sustain an acceptable power factor

for the power users. The split of the responsibilities happens at the point of common coupling (PCC), as shown in Figure 1.2.

Since the main products of all nonlinear loads are harmonic currents, which interact with the finite power system impedance to generate harmonic voltages, the harmonic currents and voltages are the problems with which power utilities and users are consistently confronted, whether in transient or steady-state. The effects of load current and source voltage harmonics are listed in Table 1-1 [15]. The IEEE-519 recommended standards for the control of harmonics are partly listed in Tables 1-2 and 1-3 [16] for the line current and the load voltage, respectively. A widely applied three-phase rectifier circuit that is shown in Figure 1.3, with its voltage and current harmonic components listed for comparison with Tables 1-2 and 1-3, shows the seriousness of the harmonic problem if the power demand is high. The current/voltage harmonic problem will be worsened when active switches such as GTOs, thyristors, power MOSFETs, MCTs, and IGBTs [17], instead of passive power diodes, are employed as rectifying switches [3, 4].

As aforementioned, it is the increasing application of power electronic circuits that causes power quality problems to power systems; it is also the application of power electronic circuits that can provide solutions for these power quality problems [18, 19, 20, 21, 22, 23, 24, 25]. With various combinations and connections of passive RLC filters and DC-to-AC inverters along the power lines or at the PCC, the power quality of power systems can be improved and brought to fit the requirements of standards. The potential of this kind of application, employing the inverters as *active filters* of power systems, has increased as the power demands of power electronic circuits in other applications have increased [26, 27, 28].

This dissertation presents a unified solution for suppressing the %THDs of both source voltage and load current with only one low-power, low-component-rating, three-

phase inverter serving as an active filter. A reduced-scale one-branch power system loaded with a three-phase diode rectifier has been built with the inverter to prove the feasibility of the solution. The power factor correction, which is the other important issue in the power system quality requirements, is a simple task once the voltage and current harmonic elimination is achieved [29]. In summary, the achievements of this dissertation include

- analysis of harmonics elimination with a low-rating 3ϕ DC-to-AC inverter,
- proof of the feasibility of harmonic elimination with a current-fed inverter,
- achievement of a low cost and simple inverter control, and
- simulation and experimental verification of the analysis.

The contents of this dissertation are organized as follows. Chapter 2 introduces the concepts of voltage/current harmonic elimination. The existing solutions for this goal and their advantages and disadvantages are also briefly discussed in this chapter. Chapter 3 discusses the operations of pulse-width-modulation (PWM) inverters which are essential for explaining the power system active filtering, including the single-phase (1ϕ) voltage-fed inverter, three-phase (3ϕ) voltage-fed inverter, and 3ϕ current-fed inverter, all of which are candidates for the role of active filter in harmonic elimination.

Chapter 4 presents the proposed low-rating solution for power system harmonic elimination (or active filtering). The mathematical model and control method are analyzed with simulation verification.

Chapter 5 is devoted to the design and test of the active filter application based on the analysis in Chapter 4. A current-fed inverter was chosen for the role of active filter in the experiment since most works of active filtering were done with voltage-fed inverters [18 - 25]. The experimental results of active filtering a reduced-scale one-branch 3ϕ power

system loaded with a 3kW diode rectifier are presented in this chapter.

Chapter 6 is the summary and conclusion of this dissertation. Appendix A contains the PSpice® circuit files for all the simulation works. Appendix B contains the MATLAB® script files for the duty-ratio and DC supply calculation of the inverter used both in the simulation and experiment.

Table 1-1. Why harmonic elimination becomes an issue.

	Transient effects	Steady-state effects
Load current distortion	• Improper operation of protection relays and circuit breakers • Amplified voltage distortion due to resonance	• Increased losses in series components of transmission/distribution and building wirings • Decreased accuracy of measuring instruments and metering
Source voltage distortion	• Improper operation of protection relays and circuit breakers • Disruption of harmonic sensitive loads	• Increased losses in parallel connected capacitors, transformers, and motors • Decreased accuracy of measuring instruments and metering

Table 1-2. IEEE-519 current distortion limits.

Maximum harmonic current in % of fundamental						
	Harmonic order(odd)					
I_{SC}/I_L	h <11	11< h <17	17< h <23	23< h <35	35< h	%THD
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	18.0

* All generators are limited to these values.
I_{SC}= Maximum short circuit current at PCC
I_L= Average maximum monthly load current
Even harmonics are limited to 25% of the odd harmonic limit above.

Table 1-3. IEEE-519 voltage distortion limits.

Maximum harmonic voltage in % of fundamental		
Bus voltage at PCC	Distortion of each harmonic	%THD
< 69 kV	3.0	5.0
69 kV - 138kV	1.5	2.5
> 139kV	1.0	1.5

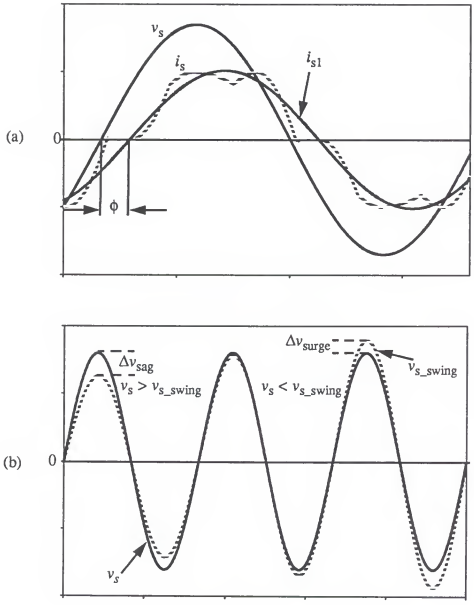


Figure 1.1. The illustration of power quality problems.
(a) Line current distortion and power factor angle.
(b) Sags and surges of line voltage.

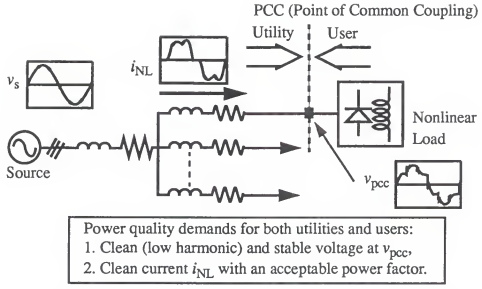
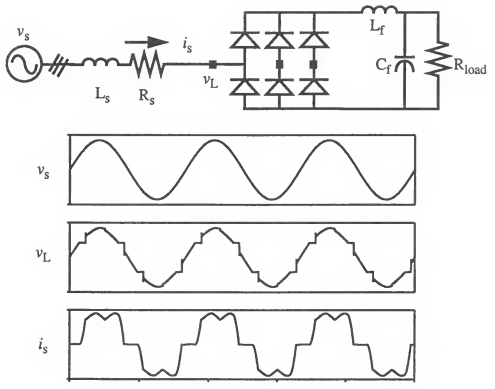


Figure 1.2. Power quality responsibilities of power utilities and users.



Harmonic component in % of fundamental					
	1st	5th	7th	11th	%THD
v_L	100	6.2	3.6	3.5	> 8.0
i_s	100	22.2	9.2	3.9	> 24.0

Figure 1.3. A typical example of the effects of nonlinear loads.

CHAPTER 2
CONCEPTS AND EXISTING SOLUTIONS OF HARMONIC ELIMINATION AND ACTIVE FILTERING

As shown in Figure 1.3, the nonlinear load generates harmonic currents which interact with the finite transmission/distribution line impedance to produce harmonic voltage along the buses and deteriorate the quality of the power system. The nonlinear load can be approximately modeled as a harmonic current source connected to the power system at the PCC as shown in Figure 2.1(a), where the load voltage and current are expressed in the fundamental terms (v_{Lf} and i_{Lf}) and the harmonic terms in summation ($\sum v_{Lh}$ and $\sum i_{Lh}$).

Note that the last subscripts of all variables concerning harmonics are denoted "$_f$" for the fundamental component and "$_h$" for the h-th order harmonic of the specific variable throughout this dissertation. To avoid confusion, the conventions for naming all variables expressed in the equations of this and following chapters are illustrated in Figure 2.2.

From Figure 2.1(a), an individual harmonic voltage at PCC is

$$v_{Lh} = -Z_s(h) \cdot i_{sh} = -Z_s(h) \cdot i_{Lh} \tag{2.1}$$

where $Z_s(h)$ is the power line impedance at the h-th harmonic frequency ($h\omega_o$):

$$Z_s(h) = R_s + j(h\omega_o)L_s \tag{2.2}$$

The source voltage v_s is assumed to contain no voltage harmonics and hence is treated as a harmonic ground.

A natural way to overcome the problem is to put a parallel (shunt) filter with impedance $Z_p(h)$ at the PCC to bypass the current harmonics from the transmission/ distribution line as shown in Figure 2.1(b). By Kirchhoff's current law (KCL), the h-th order harmonic current flow through the line will be reduced as

$$i_{sh} = \frac{Z_p(h)}{Z_s(h) + Z_p(h)} i_{Lh} \tag{2.3}$$

and the new corresponding harmonic voltage for the same load harmonic current is also reduced by the same proportion

$$\begin{aligned} v_{Lh} &= -Z_s(h) \cdot i_{sh} \\ &= -\frac{Z_s(h) \cdot Z_p(h)}{Z_s(h) + Z_p(h)} i_{Lh} \end{aligned} \tag{2.4}$$

A commonly used shunt passive filter, as shown in Figure 2.1(c), consists of three LC series-resonant filters with the corresponding corner frequencies tuned at the 5th, 7th, and 11th (high pass) order of fundamental frequency and connected to the power system at the PCC. This filter has traditionally been used to absorb load harmonic current due to its simplicity, low cost, and high efficiency.

The disadvantages of this simple power quality solution lie in its own simplicity:

(1) The passive filter's ability to absorb harmonic currents strongly depends on the power system's impedance Z_{sh}. It is difficult to design the Z_{ph} that can absorb most the current harmonics when Z_{sh} is very small. Also, from Equation (2.4), it is obvious that the first prerequisite for the shunt passive filter to work is

$$Z_s(h) + Z_p(h) \neq 0, \quad \text{for all } h \tag{2.5}$$

to avoid resonance at any h-th order of fundamental frequency.

(2)The filter strongly interacts with the utility and other loads in the vicinity, and its design is sensitive to component tolerance [25].

(3) If the source voltage v_s contains harmonics, such as the case of a bus loaded with other nonlinear loads, the passive filter at the PCC of a specific load cannot suppress the harmonic voltage from the bus and may be overloaded.

(4) When the power factor does not require correction, the phase-leading fundamental current (i_{pf} for the fundamental angular frequency ω_o) through the filter may cause a leading power factor that exceeds the acceptable range and may pose a stability problem to the power system.

$$i_{pf} \approx j\omega_o (C_5 + C_7 + C_H) \cdot v_{Lf} \tag{2.6}$$

To overcome the disadvantages of the shunt passive filter but retain its advantages, various passive/active filter combinations have been explored and put into practical applications.

There are three possible types of filter combinations:

(1) An active filter in series with the power system and a shunt passive filter connected to load at the PCC,

(2) An active filter in series with the passive filter connected to load at the PCC, and

(3) Combination of (1) and (2), one active filter in series with the power line and one active filter in series with the passive filter connected to load at the PCC.

The characteristics of the above three combinations are briefly introduced in the

following sections.

2.1. Active Filter in Series with Power Line and Shunt Passive Filter

An active filter (switching-mode DC/AC inverter) in series with the distribution line [20, 21, 25, 30, 31] can block the source voltage harmonics to prevent overloading the shunt passive filter at the PCC. The schematic sketch of this combination and the equivalent circuit diagram are shown in Figures 2.3 and 2.4(a), respectively.

All the filters applied to the power system bear one goal as stated in the power quality requirements in Chapter 1: to keep only the fundamental voltage and current with an acceptable power factor in the system by suppressing the harmonics of power line current and load point voltage. The merits of all the filter combinations should be evaluated under this premise. This series active and shunt passive filter combination can block the source voltage harmonics and make the line current i_s contain only fundamental component i_{sf} by generating a harmonic voltage v_{ih} in series with the power line as

$$\sum_{h \neq 1} v_{ih} \equiv \sum_{h \neq 1} v_{sh} - v_{Lh} \tag{2.7}$$

In this case, the power line is open to harmonic currents as shown in Figure 2.4(b). Because the load current harmonic Σi_{Lh} will all flow through the shunt passive filter and produce harmonic voltages at the PCC as

$$\sum_{h \neq 1} v_{Lh} = - \sum_{h \neq 1} Z_p(h) \cdot i_{Lh} \tag{2.8}$$

Each individual voltage harmonic v_{Lh} is strongly dependent on the impedance Z_p of the shunt passive filter at each different harmonic to determine whether it is tolerable. Furthermore, if the passive filters are identical for both Equations (2.4) and (2.8), the PCC

harmonic voltage for this combined filter is not much different from the one with only the passive filter. This combined filter has no way to get rid of the voltage harmonics at the PCC because of the fact that the passive filter impedance $Z_p(h)$ cannot be zero. The only advantage is that the constraint of Equation (2.5) is removed and the design of $Z_p(h)$ can be done only according the tolerable voltage harmonics at the PCC when the overall dynamics of the combined filter are not concerned. Even though the line impedance $Z_s(h)$ is not involved in the design of the passive filter $Z_p(h)$, it is still very critical and sensitive to the component tolerances.

The series inverter is well suitable for compensating the unbalanced source voltages [30] and for the role of uninterruptible power supply (UPS) [31, 32] in case a large source sag or short circuit happened. If the source voltage is balanced and does not have harmonics, the series inverter is capable of filtering the line current harmonics (%THD of i_s) only but has no effect on the voltage harmonics (%THD of v_L) at the PCC and the phase-leading fundamental current in the passive filter. Also, the overall power (VA) ratings and the ratings of individual components of the inverter must be high enough to accommodate the full load current passing through its circuitry; hence the losses in the inverter will be high and the efficiency will be low.

2.2. Active Filter in Series with Shunt Passive Filter

This combination connects a passive filter in series with an active filter to the PCC in parallel with the nonlinear load as schematically shown in Figure 2.5 [18, 23, 24, 33, 34, 35, 36, 37]. The equivalent circuit diagram is shown in Figure 2.6(a).

For the power quality responsibilities, the power utilities need only to keep the voltage at the PCC a stable fundamental, and the users need only to block the load current harmonics to flow into the power line. If the two requirements are met, for the specific user, the utility cannot blame the user for the current harmonics in the power lines and the user cannot ask the utility to fix the voltages at other buses. The two requirements are actually one: by just keeping a stable fundamental voltage at the PCC with this combined filter in Figure 2.5, no current harmonics from the load can flow into the power line if the source bus voltage is harmonic free.

In this scheme, the same current passes through the passive and the active filters. If the active filter generates a voltage (Σv_{ih}) equal in amplitude but out of phase to the harmonic voltage (Σv_{ph}) across the passive filter caused by the current, the voltage v_L at the PCC will be fundamental v_{Lf} only.

$$\begin{aligned} v_L &= v_p + v_i \\ &= \left(v_{pf} + \sum_{h \neq 1} v_{ph}\right) + \sum_{h \neq 1} v_{ih} \\ &= \left[v_{pf} + \sum_{h \neq 1} Z_p(h) \cdot (-i_{Lh})\right] + \sum_{h \neq 1} Z_p(h) \cdot i_{Lh} \\ &= v_{pf} + \sum_{h \neq 1} Z_p(h) \cdot (-i_{Lh} + i_{Lh}) \\ &= v_{pf} \\ &= v_{Lf} \end{aligned} \tag{2.9}$$

The active filter acting in this way makes the series active/passive filters a short circuit for the harmonic current and the PCC a harmonic ground as shown in Figure 2.6(b).

In this filter combination, if there are no harmonics presented in the source voltage v_s, the line current i_s will contain the fundamental components of the load current i_{Lf} and the filter current i_{pf}. If there are harmonics Σv_{sh} in the source voltage v_s, at the price of

increasing the ratings of the filters, this combined filter still can absorb the harmonic current generated by Σv_{sh} and keep the voltage at the PCC fundamental only.

$$\sum_{h \neq 1} i_{sh} = \sum_{h \neq 1} \frac{v_{sh}}{Z_s(h)} \tag{2.10}$$

$$\sum_{h \neq 1} v_{ih} = -\sum_{h \neq 1} Z_p(h)\ (i_{sh} + i_{Lh}) \tag{2.11}$$

Theoretically, this combined filter can remove any voltage harmonics at the bus (PCC) it is connected to, but it cannot remove the line current harmonics Σi_{sh} generated from other buses (source bus in this case). However, these current harmonics are not the responsibility of the load and should be taken care of by the same hybrid filter at the source bus to make the source voltage free of harmonics, if the source bus is connected to other important loads.

Depending on the configurations of inverters in the role of the active filter, this hybrid filter can work even in a situation when the source voltage v_s is slightly unbalanced. Suppose that the 3ϕ source voltages are unbalanced as

$$\begin{aligned} v_{asf} &= v_{sf} + \Delta v_{asf} \\ v_{bsf} &= v_{sf} + \Delta v_{bsf} \\ v_{csf} &= v_{sf} + \Delta v_{csf} \end{aligned} \tag{2.12}$$

which cause the PCC voltages to become

$$\begin{aligned} v_{aLf} &= v_{Lf} + \Delta v_{aLf} \\ v_{bLf} &= v_{Lf} + \Delta v_{bLf} \\ v_{cLf} &= v_{Lf} + \Delta v_{cLf} \end{aligned} \tag{2.13}$$

where Δv is the small fundamental voltage variation in the corresponding phases. The inverter can generate a fundamental voltage besides all the voltage harmonics as

$$\begin{aligned} v_{ai} &= \Delta v_{asf} \\ v_{bi} &= \Delta v_{bsf} \\ v_{ci} &= \Delta v_{csf} \end{aligned} \tag{2.14}$$

to counteract the unbalanced 3ϕ voltages and keep the voltages at the PCC well balanced. With both of the source fundamental voltage variations and voltage harmonics presented, the line current i_s will be balanced yet contain harmonics while the active filter generates the counteracting fundamental and harmonic voltages.

Note that the active filter is only able to compensate the unbalanced 3ϕ voltages for a small range of Δv_{sf}. Since the unbalanced 3ϕ voltages would require the inverter to provide high fundamental current flowing back to the source bus, which is beyond the inverter's ability as an active filter and other better measures can be used [27, 38]. It is impractical for the shunt active filter (inverter) to act the role of UPS when the source voltage has a large sag/surge or short circuit. When the active filter is designed with UPS ability, a fast-acting solid-state circuit breaker [39] must be inserted in the power line to isolate the source bus when faults (large sags/surges or short circuit) happen.

Although this hybrid filter is the most versatile one and can achieve the power quality requirements at the PCC, because conventionally the LC passive filters are tuned at 5th, 7th, and higher harmonics, the current flowing through the active filter contains a significant fundamental component even when the compensation of unbalanced fundamental voltages are not required. The overall power and component ratings of the active filter still must be high to accommodate the fundamental current; hence the losses in the active filter will be high, too. The phase-leading fundamental current still imposes the constraint for design of the passive filter as mentioned in Section 2.1.

2.3. Active Filters in Series with Power Line and in Series with Shunt Passive Filter

This configuration [27, 38] is the combination of the filters in Sections 2.1 and 2.2 as shown in Figure 2.7. The active filter in series with the power line takes care of the source voltage harmonics and the fundamental voltage variations to make the line current i_s balanced three-phase only as mentioned in Section 2.1. The other active filter in series with the passive filter at the PCC absorbs all load current harmonics and keeps the PCC voltage balanced three-phase only as described in Section 2.2.

For the purpose of harmonic elimination only, the active filter in series with the power line actually can be considered redundant since it cannot solve the source voltage problems for other loads connected to the bus, and the power losses and ratings for the series active inverter are high because of the full fundamental load current flowing through its circuitry.

A better filter combination can be employed to reduce the power losses caused by the fundamental current circulating in the shunt active filter and will be introduced in Chapter 4. Detailed operating descriptions for both voltage-fed and current-fed inverters in the position of active filter to generate the required harmonic voltages are included in this chapter, too. In order to explain the operational principals of an active filter which generate a voltage containing many frequencies, the single frequency operations of PWM inverters, both voltage-fed and current-fed, are described in Chapter 3.

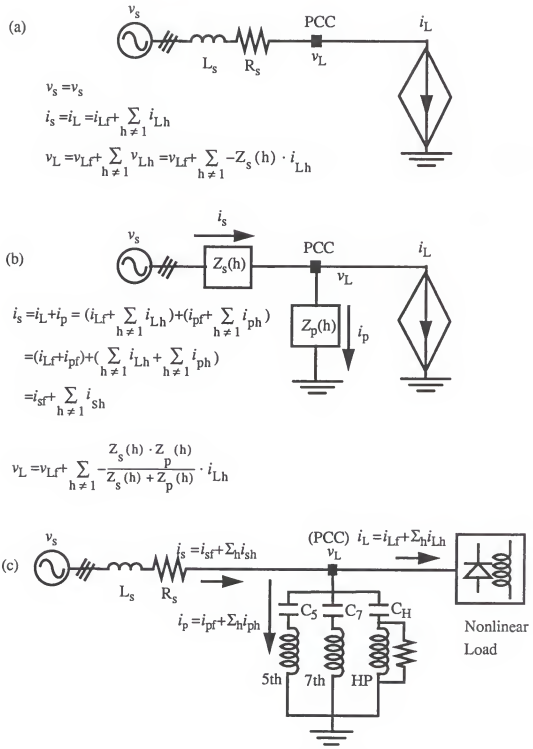
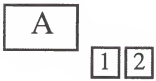


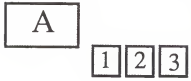
Figure 2.1. The schematic sketch of a power system with nonlinear load
(a) the load modeled as a current source;
(b) a parallel passive filter Z_{ph} connected to the PCC;
(c) a commonly applied filter bank as Z_{ph}.

1. For voltage and current variables with two subscripts:



A: "v" for voltage
"i" for current
1: "L" for load
"i" for active filter
"p" for passive filter
"s" for source
2: "f" for fundamental
"h" for h-th order of harmonic

2. For voltage and current variables with three subscripts:



1: "a", "b", and "c" for respective phases
2: "L" for load
"i" for active filter
"p" for passive filter
"s" for source
3: "f" for fundamental
"h" for h-th order of harmonic

3. For impedance variables:

Z: for impedance
1: "L" for load
"p" for passive filter
"s" for source line
n: "f" for fundamental
"h" for h-th order of harmonic

Figure 2.2. Conventions for the variable notations used in the discussion of harmonic elimination.

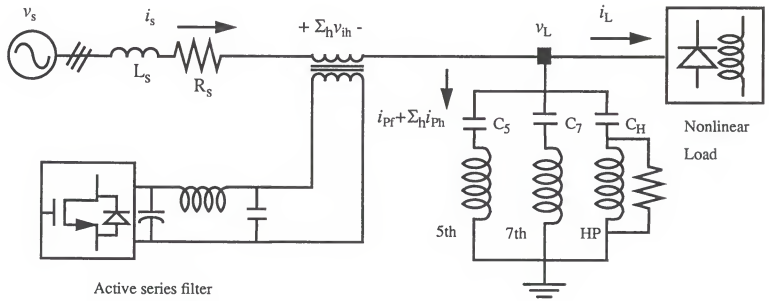


Figure 2.3. The schematic sketch of hybrid active/passive filters: the active filter in series with the power line and the passive one connected to the load at the PCC.

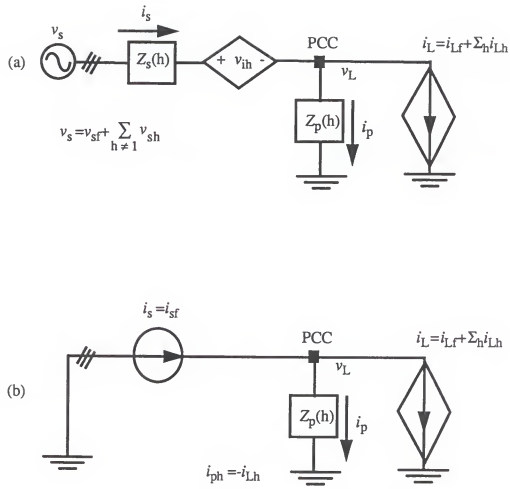


Figure 2.4.The equivalent circuit diagram of the hybrid active/passive filters in Figure 2.3 (a) and the function of the active filter (b).

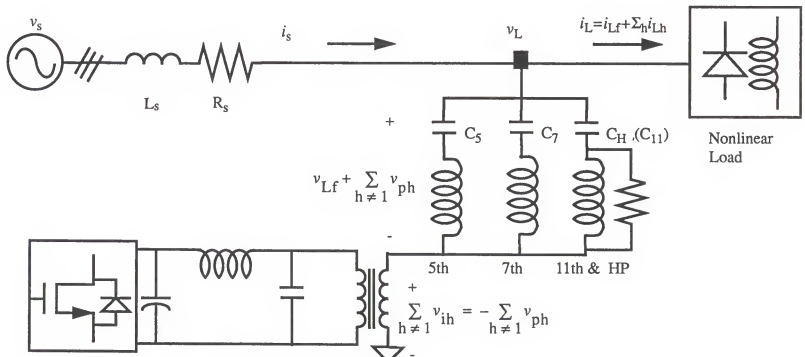


Figure 2.5. The schematic sketch of hybrid active/passive filters: the active filter in series with the passive one and in parallel with the load at the PCC.

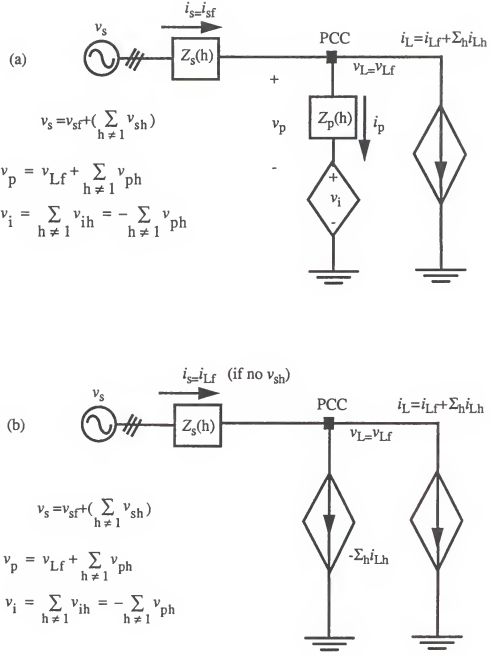


Figure 2.6. The equivalent circuit diagram of the hybrid active/passive filters in Figure 2.5 (a) and the function of the active filter (b).

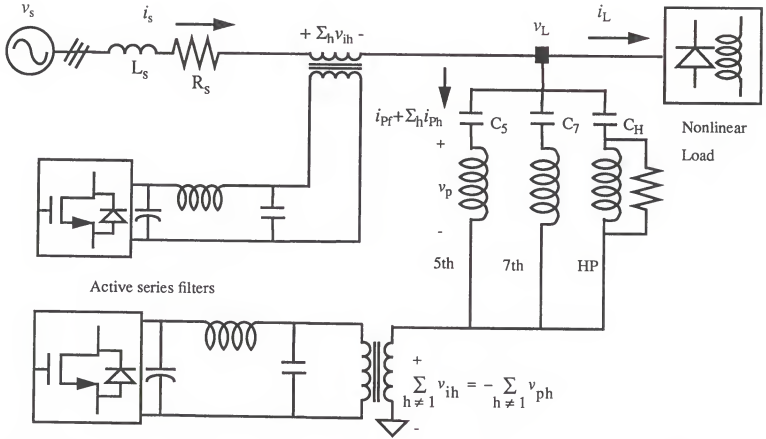


Figure 2.7. The schematic sketch of hybrid active/passive filters: one active inverter in series with the power line and the other in series with the passive filter connected in parallel with the load at the PCC.

CHAPTER 3
OPERATIONS OF PULSE-WIDTH-MODULATED INVERTERS

3.1. Introduction to Power Electronic Converters

There are various types of power electronic converters for different functions and operational requirements, and with the growing development in power semiconductor industry, the possibilities of new applications for existing converters and inventions of new converters are virtually limitless. The basic constituents of a power electronic converter are (1) the input, (2) the output, and (3) the power conversion circuitry (switch-array) as schematically shown in Figure 3.1.

The power conversion circuitry, or switch-array, is the main body of a power electronic converter. This circuitry serves as an interface between various input sources and output loads to achieve any imposed performance requirement. With different power sources and loads, and different positions the source and load place on the switch-array, power electronic converters can be classified into the following four categories

(1) DC-to-DC (DC/DC, converters),

(2) DC-to-AC (DC/AC, inverters, 1ϕ or 3ϕ),

(3) AC-to-DC (AC/DC, rectifiers), and

(4) AC-to-AC (cycloconverters, frequency changers)

as shown Figure 3.1. The active filter discussed in this dissertation is one of the applications of the DC/AC converter, which is conventionally called an inverter.

Depending on whether the DC supply is a voltage source or a current source [2, Chapters 4 and 5], the inverters can be further classified as

- voltage-fed inverters, and
- current-fed inverters [40,41,42].

Figures 3.2(a) and 3.2(b) show the two types of inverters in single-phase applications.

The formation of switch-arrays and the control are different for the voltage-fed and current-fed inverters. For a 1ϕ voltage-fed (full-bridge) inverter, the switch-array is composed of two *single-pole-double-throw* switches (1P2T) S_{11}-A-S_{12} and S_{21}-B-S_{22}, where S_{11}/S_{12} are the two throws associated with pole A, and S_{21}/S_{22} are the two throws associated with pole B, as labeled in Figure 3.2(a).

The "S_{mn}" labelling convention for the switch throw is that the first subscript "$_m$" denotes the pole and the second subscript denotes a throw. Both "$_m$" and "$_n$" can be numerical or alphabetical depending on the types of inverters and one's preferences.

Due to the fact that the voltage source V_{dc} of the inverter cannot be short circuited and the current i_L through the output filter inductor L must be continuous, one and only one of the two throws (S_{11}/S_{12} and S_{21}/S_{22}) in each switch branch must conduct at any instant. Either S_{11} is ON and S_{12} is OFF, or vice versa. The same control restriction also applies to S_{21}/S_{22}. Besides the above restrictions and the limitations imposed by the physical power electronic switches, the two switch branches can be independently controlled to achieve any required 1ϕ output [43, 44, 45, 46, 47, 48]. With the same control restrictions as a 1ϕ inverter, the switch-array of a 3ϕ voltage-fed inverter is composed of three *single-pole-double-throw* switch branches (1P2T x3) S_{a1}-A-S_{a2}, S_{b1}-B-

S_{b2}, and S_{c1}-C-S_{c2} as shown in Figure 3.3(a), where S_{a1}/S_{a2}, S_{b1}/S_{b2}, and S_{c1}/S_{c2} are the throws associated with the poles A, B, and C, respectively. The "$_a$", "$_b$", and "$_c$" in the throw labels denote the poles which are coincident with the conventional notations for three-phase power systems, and the "$_1$" and "$_2$" denote the specific throws.

The characteristics of the voltage-fed inverter switch-array can be summarized as

(1) The basic constituent is always a *single-pole-double-throw* switch branch; the number, N, of switch branches (1P2T xN) employed in a switch-array depends on the phases or the specific applications of the inverter. There are two branches (1P2T x2) in the switch-array for 1ϕ applications and three branches (1P2T x3) in the switch-array for balanced 3ϕ applications.

(2) The two throws of a switch are connected to the two terminals of the voltage source, respectively.

(3) The poles are in the middle of branches and connected to loads.

All theses characteristics are illustrated in Figure 3.3(a).

For a 1ϕ current-fed inverter, the two *single-pole-double-throw* branches in the switch-array is X-S_{11}-S_{12} and Y-S_{21}-S_{22}, where X and Y are the poles and S_{11}/S_{12} and S_{21}/S_{22} are the throws of the switches, as shown in Figure 3.2(b). The switches are grouped in this way to reflect the fact that the current source, represented by the current through the inductor L, I_{dc}, must be continuous and cannot be open circuited. The current-fed inverter must be operated under the restrictions that, at any instant, at least one throw of each switch branch, X-S_{11}-S_{12} and Y- S_{21}-S_{22}, must be ON to ensure the continuity of the current I_{dc}. For a 3ϕ inverter [41 - 43, 48], the switch-array is composed of two *single-pole-triple-throw* switches (1P3T x2) X-S_{1a}-S_{1b}-S_{1c} and Y-S_{2a}-S_{2b}-S_{2c} as shown in Figure

3.3(b), where the $S_{1a}/S_{1b}/S_{1c}$ and $S_{2a}/S_{2b}/S_{2c}$ are the throws associated with the poles **X** and **Y**, respectively. The "$_1$" and "$_2$" in the throw labels denote the poles, and the "$_a$", "$_b$", and "$_c$" denote the specific throw to keep the conventional 3ϕ notations. Under normal operation, one throw from each switch is ON at any instant.

The characteristics of current-fed inverters, as illustrated in Figure 3.3(b), can be summarized as

(1) There are only two *single-pole-N-throw* switches (1PNT x2) in a current-fed inverter, where "N" is the number of phases of the inverter or is set by specific applications; for a 1ϕ inverter N= 2 and for a balanced 3ϕ inverter N=3.

(2) The two poles of the two switch-branches are connected to the two terminals of the current source, respectively.

(3) Two throws, each from one of the switches, are connected to the loads as the output nodes for the inverter.

The difference in the positions of poles determines the different PWM operation modes for voltage-fed and current-fed inverters. The various operations of a widely employed 1ϕ voltage-fed inverter known as the full-bridge inverter is described in detail in Section 3.2. The operations introduced in this section give the operational basis of all inverters. Section 3.3 continues Section 3.2 to introduce the PWM operations of a 3ϕ voltage-fed inverter, and Section 3.4 describes the PWM operations of a 3ϕ current-fed inverter. When an inverter is not required to deliver power to a load, but only to accommodate certain current and produce certain voltage in a range of the frequency spectrum, the inverter is operated as an *active filter*, which is the main topic of this dissertation and is described in later chapters.

3.2. Operations of Full-Bridge Inverter

Other than active filtering, the full-bridge inverter is widely employed in various applications such as photovoltaic-utility interfaces [49], motor drives [2 - 4], and uninterrupted power systems (UPS) [31, 50, 51]. The physical devices for the switch throws are semiconductor devices such as GTOs, thyristors, power BJTs, power MOSFETs, MCTs, and IGBTs. A full-bridge inverter with power MOSFETs as the switch throws (or switches) connected to the switching poles labeled as **A** and **B** is shown in Figure 3.4. The common application of the inverter is to generate a stable sinusoidal output voltage for delivering power to various loads. For this application, the switches are commonly controlled by a variety of PWM techniques and by phase-shifted square-wave drives [2 ~ 4].

3.2.1. The Phase-Shifted Square-Wave Drives

In phase-shifted square-wave drives, the switches S_{11}/S_{12} and S_{21}/S_{22} are commutated at the output frequency to generate square waves at **A** and **B** whose phases are shifted to control the amplitude of $v_{\mathbf{AB}}$ as shown in Figure 3.5. The advantages of phase-shifted square-wave drives are (1) the drive control is simple and (2) the switching losses are low. However, the high contents of low-order harmonics in the voltage profile prevent this driving method from being universally applied. Only in the case of very high power application (> hundreds of kilowatts) where the semiconductor technology has not advanced enough to have switches switched at high frequencies, this method is applied with some modifications to eliminate certain low-order voltage harmonic components and, in fact, becomes a special type of PWM drive [45 - 47].

3.2.2. The PWM Operations

In PWM techniques, all switches are usually commutated at a frequency higher than the output frequency so that the switching harmonics are moved to high frequency and can be filtered more easily. Thus, the output voltage can be made a high quality sinusoidal waveform with very small harmonic contents [52], at the expense of much higher switching losses than the phase-shifted square-wave drives. Commonly used PWM techniques are sinusoidal PWM, "over-modulated" PWM, and selective-harmonic-elimination PWM [45 - 47]. In these techniques, a modulation waveform (*m*) is compared with a carrier waveform (*c*) to determine the switching pattern. The resulting harmonic spectra are usually sensitive to the carrier waveform, usually a ramp or a triangular waveform, as well as to the ratio of the switching frequency to modulation frequency. In order to introduce these PWM operations without confusion and redundance, the nomenclature for explaining the PWM methods is listed in Table 3-1.

There are three types of modulation for both sinusoidal PWM and over-modulated PWM:

(1) bipolar PWM (BPWM),

(2) unipolar PWM (UPWM) [3, Chapters 8], and

(3) hybrid PWM (HPWM) [44].

The only difference between the sinusoidal PWM and over-modulated PWM lies in the amplitude modulation ratio, m_a, which results in different harmonic spectra. For the sinusoidal PWM

$$m_a = \frac{\max(m)}{\max(c)} \leq 1 \qquad (3.1)$$

This is also called the linear modulation PWM mode. For the over-modulated PWM

$$m_a = \frac{\max(m)}{\max(c)} > 1 \tag{3.2}$$

The other key index in PWM is the frequency modulation ratio, m_f, defined as

$$m_f = \frac{f_s}{f_o} \tag{3.3}$$

The inverter operated under the linear modulation mode is introduced in detail with the HPWM method. The differences among the switching characteristics of linear modes BPWM, UPWM, and HPWM are discussed later in this section.

3.2.3. HPWM Waveforms

The hybrid PWM method separates the four switches of a full-bridge inverter into two groups: one is fast switched at the PWM frequency f_s and the other is slowly switched at the output frequency f_o. In general, any two of the four switches in the inverter, shown in Figure 3.4, can be operated at the output frequency f_o, and the other two pulse-width-modulated at high frequency f_s. For simplicity, S_{21} and S_{22} are assigned the role of the slow switches, and S_{11} and S_{22} the role of the fast (PWM) switches. Since S_{21} and S_{22} are switched at low frequency, their switching losses are greatly reduced. The HPWM switch operation is illustrated in Figure 3.6. It will be shown later that the effective duty ratio d_e is proportional to the low-frequency components of the output voltage v_o. Thus, for the following discussion,

$$d_e \sim v_o \tag{3.4}$$

One can expect that because of the LC filter, the output voltage v_o is generally "smooth" and only contains the low-frequency components of the bridge output voltage v_{AB} which is a PWM waveform. An efficient way to synthesize a positive (negative) v_o would employ only positive (negative) and zero pulses in v_{AB}. This can be accomplished by turning on only S_{22} in the S_{21}/S_{22} switch pair when $v_o > 0$, and by turning on only S_{21} when $v_o < 0$. Thus, S_{21} and S_{22} are switched at the output frequency f_o, which is generally low. The switching functions of S_{21} and S_{22} are

$$\begin{aligned} s_{21} &= 1, \quad d_e < 0 \\ s_{21} &= 0, \quad d_e > 0 \end{aligned} \tag{3.5}$$

$$s_{22} = 1 - s_{21} \tag{3.6}$$

If the negative terminal of V_{dc} is used as the circuit common, the voltage at node B is

$$v_B = s_{21} V_{dc} \tag{3.7}$$

To synthesize a sinusoidal v_o, the switch pair S_{21}/S_{22} needs to be driven by a pulse-width modulator. A typical pulse-width modulator receives as input a carrier waveform c and a modulation waveform m and outputs a switching function p according to

$$\begin{aligned} p &= 1, \quad m > c \\ p &= 0, \quad m < c \end{aligned} \tag{3.8}$$

An HPWM full-bridge inverter is equivalent to two buck DC-DC converters, one for each polarity of d_e or v_o. The common connection of the buck DC-DC converters is node B. When $d_e > 0$, B is connected to the negative terminal of V_{dc} via S_{22}. A "positive" buck converter results with V_{dc} as input, S_{11} as the active switch with duty ratio d_e, and

S_{12} as the "diode." When $d_e < 0$, B is connected to the positive terminal of V_{dc} via S_{21}. A "negative" buck converter results with $-V_{dc}$ as input, S_{12} as the active switch with duty ratio $-d_e$, and S_{11} as the "diode." Thus, the switching functions of S_{11} and S_{12} are

$$\begin{aligned} s_{11} &= p, \quad d_e > 0 \\ s_{11} &= 1 - p, \quad d_e < 0 \end{aligned} \tag{3.9}$$

$$s_{12} = 1 - s_{11} \tag{3.10}$$

The voltage at node A is then

$$v_A = s_{11} V_{dc} \tag{3.11}$$

If the frequency of c is much higher than the frequency of m, the low-frequency components of p satisfies

$$\bar{p} \approx m \tag{3.12}$$

where in HPWM,

$$m = |d_e| \tag{3.13}$$

From Equations (2.3) and (3.11),

$$v_{AB} = (s_{11} - s_{21}) V_{dc} \tag{3.14}$$

From Equations (3.5), (3.9), and (3.14)

$$\begin{aligned} v_{AB} &= pV_{dc}, \quad d_e > 0 \\ v_{AB} &= -pV_{dc}, \quad d_e < 0 \end{aligned} \tag{3.15}$$

From Equations (3.12), (3.13), and (3.15), and the observation that $v_{AB} \approx v_o$,

$$v_o \approx \bar{v}_{AB} = d_e V_{dc}, \quad |d_e| < 1 \tag{3.16}$$

The preceding equation is the synthesis rule for HPWM. Note that d_e can contain low-order harmonics to synthesize low-order harmonics for v_o of an active filter.

3.2.4. HPWM Inverter Operation

During the course of operation, the HPWM converter transforms into a positive buck converter when $d_e > 0$ and a negative buck converter when $d_e < 0$. As long as $d_e > 0$, S_{22} is turned on and the positive buck converter shown in Figure 3.7(a) results. During d_e/f_s, $d_e > 0$, S_{11} is on and the positive buck converter becomes the switched circuit in Figure 3.7(b). During the remainder of the switching period, S_{12} is on and the switched circuit shown in Figure 3.7(c) results. If d_e is quasi-dc, $v_o = d_e V_{dc}$ ($d_e > 0$).

As long as $d_e < 0$, S_{21} is turned on and the HPWM inverter is essentially a negative buck converter as shown in Figure 3.7(d). Switch S_{12} is turned on for $-d_e/f_s$ and switch S_{11} is turned on for the remainder of the switching period. If d_e is quasi-dc, $v_o = -d_e(-V_{dc}) = d_e V_{dc}$ ($d_e < 0$). Thus, $v_o = d_e V_{dc}$, regardless of the sign of d_e. If d_e is sinusoidal, so is v_o.

Figure 3.8 shows the PSpice® simulated waveforms for d_e, v_o, and the currents in S_{11} and S_{21}. As expected, v_o is essentially proportional to d_e. The current in S_{21} varies at the frequency of d_e, i.e., slowly. The current in S_{11} is switched at the carrier frequency. The envelope of this current is the current through the inductor i_L in Figure 3.4.

3.2.5. HPWM Inverter Analysis.

The low-frequency behavior and the modeling technique of a fast-switching PWM converter have been well studied [40, 41, 43, 44]. Using this technique and Equation

(3.16), one can derive the following state-space equations describing the low-frequency performance of the HPWM inverter

$$L \cdot \frac{di_L}{dt} = -v_o + d_e V_{dc} \tag{3.17}$$

$$C \cdot \frac{dv_o}{dt} = -\frac{1}{R} \cdot v_o + i_L \tag{3.18}$$

The above equations can be used to determine d_e for synthesis of a given v_o. Let v_o be sinusoidal and in the form of

$$v_o(t) = V_m \sin(\omega_o t) \tag{3.19}$$

Then d_e can be found by substitution of Equation (3.19) into (3.17) and (3.18):

$$d_e(t) = \sqrt{\left[1 - \left(\frac{\omega_o}{\omega_c}\right)^2\right]^2 + \left(\frac{1}{Q}\frac{\omega_o}{\omega_c}\right)^2} * \frac{V_m}{V_{dc}} \sin\left(\omega_o t + \tan^{-1}\frac{(1/Q)\ (\omega_o/\omega_c)}{1 - (\omega_o/\omega_c)^2}\right) \tag{3.20}$$

$$-1 \le d_e(t) \le 1$$

where

$$\omega_c = \frac{1}{\sqrt{LC}} \qquad Q = \frac{R}{\omega_c L} \tag{3.21}$$

and the current through the inductor L is

$$i_L(t) = \frac{V_m}{R}\sqrt{1 + \left(Q\frac{\omega_o}{\omega_c}\right)^2} * \sin\left(\omega_o t + \tan^{-1}\left(Q\frac{\omega_o}{\omega_c}\right)\right) \tag{3.22}$$

Although the above derivations are for the low-frequency behavior of HPWM, it can be proven [3, Chapter 8] that BPWM and UPWM have the same low-frequency

behavior as HPWM. Hence, Equations (3.17) to (3.22) are applied to all BPWM, UPWM, and HPWM inverters in the linear-modulation mode.

3.2.6. The Output Characteristics of BPWM, UPWM, and HPWM

Although the low-frequency behavior of BPWM, UPWM, and HPWM are identical, the switching pattern and the characteristic voltage v_{AB} of sinusoidal BPWM, UPWM, and HPWM are different as shown in Figures 3.9(a), 3.9(b), and 3.9(c), respectively. The PWM method faces the same harmonics problem as the phase-shifted square-wave drives if the carrier frequency is not significantly higher than the modulation frequency (generally $m_f < 15$). Under this circumstance, the differences between the three modulations appear and their frequency spectra need to be identified so that the appropriate steps to deal with the undesirable harmonics may be taken.

As shown in Figure 3.9(a.1), in BPWM, S_{11} and S_{22} are turned on and off together by a single pulse-width modulator and a single modulation waveform. Consequently, v_{AB} contains both positive and negative pulses in the positive (or negative) half cycle of m as shown in Figure 3.9(a.2).

In UPWM, each switching pole is driven by its own pulse-width modulator. The modulation functions for the two pulse-width modulators are out-of-phase as illustrated in Figure 3.9(b.1). Consequently, only positive (negative) and zero pulses are present in the positive (negative) half cycle of m. In addition, the use of out-of-phase modulation functions for the switching poles effectively *doubles* the switching frequency, as is evident in Figure 3.9(b.2). Thus, although $m_f = 9$ in Figure 3.9(b.1), the effective frequency modulation ratio found in v_{AB} is

$$m'_f = 2m_f = 18 \tag{3.23}$$

Note that the UPWM m'_f has been selected to equal the HPWM m_f (Figure 3.9(c.1)).

A comparison between Figures 3.9(b.2) and 3.9(c.2) suggests that for triangular carriers, HPWM and UPWM generate identical v_{AB} and, hence, identical frequency spectra for v_{AB}. This is because the HPWM modulation and carrier waveforms in Figure 3.9(c.1) are the rectified UPWM modulation and carrier waveforms in Figure 3.9(b.1). Thus, there is no need to derive the frequency spectrum for HPWM with a triangular carrier since the frequency spectrum for UPWM with a triangular carrier has been given [3, 53].

The v_{AB} frequency spectra of HPWM and UPWM are shown in Figure 3.10(a) and 3.10(b), respectively, for triangular carriers. Since the v_{AB} of HPWM and UPWM has odd symmetry ($v_{AB}(-t) = -v_{AB}(t)$) and half-wave symmetry ($v_{AB}(t+1/2f_s) = -v_{AB}(t)$), only odd harmonics are present. The UPWM harmonic orders for a triangular carrier are [3, Chapter 8]

$$h_{UPWM} = jm'_f \pm k \quad , \text{ even } m'_f, \text{ odd } k \tag{3.24}$$

For each harmonic order h_{UPWM} determined by the set (j,k), there is a corresponding HPWM harmonic order h_{HPWM} with the same amplitude:

$$h_{HPWM} = jm_f \pm k \quad , \text{ even } m'_f, \text{ odd } k \tag{3.25}$$

The harmonic amplitude calculation of v_{AB} of UPWM has been presented in literature [3, 52] hence is not repeated in this section.

Figures 3.11(a) and 3.11(b) show the harmonic spectra for HPWM and UPWM, respectively, for ramp carriers. It can be observed that the *frequency-doubling* effect in the UPWM waveform is lost. This is because the ramp carrier does not possess half-wave symmetry, and its rectification is a triangular carrier of the same frequency. The hybrid PWM generates less sidebands than UPWM. The maximum harmonic amplitude of HPWM appears to be lower than that of UPWM.

The harmonic spectrum of BPWM with a triangular carrier is shown in Figure 3.12 for comparison. Although BPWM is simpler to implement, and thus is more popular, than HPWM and UPWM, its harmonics are more difficult to filter.

In summary, if the quality of the output voltage v_{AB} is measured by the harmonic spectrum and the switching losses, the quality of HPWM is insensitive to the shapes of carriers. When triangular carriers are employed, the qualities of HPWM and UPWM with half the carrier frequency are identical, and are superior to the quality of BPWM. With ramp carriers employed, the HPWM spectrum is comparable to the UPWM and still superior to the BPWM spectra, but has only half the switching losses of the later two. Furthermore, since HPWM allows two of the four switches in a full-bridge inverter to operate at low (output) frequency, slower semiconductor devices can be used in the positions of slowly switched switches, which reduces not only the switching losses but also the conduction losses.

Except for the sinusoidal PWM, the HPWM, UPWM, and BPWM are also applied to other PWM techniques, as well as "soft" PWM [53], and 3ϕ applications. For instance, with the mixture of fast and slow switches in the same converter, the "six-step" PWM [43] may be considered an implementation of HPWM in three-phase inverters.

3.3. Operations of Three-Phase Voltage-Fed Inverter

A three-phase (3ϕ) voltage-fed inverter with power MOSFETs as the switches is shown in Figure 3.13. The output capacitor and load in each phase are assumed to be the same for a balanced 3ϕ system. The inverter in Figure 3.13 provides 3ϕ *line-to-line* voltages to the Y-Y connected capacitor bank and load [54, 55, 56]. The only difference between a Δ-Δ connected load and a Y-Y connected load is that the output voltages provided by the inverter become the *phase-to-phase* voltages in a Δ-Δ connection, instead of *line-to-line* voltages in Y-Y connection, but there is no effect on the analysis of the way an inverter operates. The square-wave drives in the 1ϕ inverter can still be applied to the 3ϕ inverter [4, Chapter 10] with the same harmonic problem. For a high quality output, PWM and its variations [40 - 48, 57, 58] are the choices.

The 3ϕ voltage-fed inverter, as redrawn in Figure 3.14 with all the MOSFETs replaced by three 1P2T switch branches, can be analyzed by the state-space method [59, 60, 61, 62]. Under the quasi-dc duty-ratio assumption [40, 41], the differential equations for the low-frequency behavior of the inverter can be obtained and the low-frequency values of the states can be calculated by state-space averaging after performing *d-q* or *o-f-b* transformation to change the state-space equations from the time-varying reference frame to a stationary reference frame [41, 43, 54 -56].

In Figure 3.14, s_{a1}/s_{a2}, s_{b1}/s_{b2}, and s_{c1}/s_{c2} are the switching functions of switches S_{a1}/S_{a2}, S_{b1}/S_{b2}, and S_{c1}/S_{c2}, and d_{a1}/d_{a2}, d_{b1}/d_{b2}, and d_{c1}/d_{c2} are the corresponding duty ratios of the switching functions, as defined in Table 3-1. The relationship between the corresponding s_{a1}/s_{a2}, s_{b1}/s_{b2}, and s_{c1}/s_{c2} and d_{a1}/d_{a2}, d_{b1}/d_{b2}, and d_{c1}/d_{c2} can be illustrated in Figure 3.15. While a switching function "s" is always "1" or "0" representing

the ON or OFF state of the switch throw, respectively, the duty-ratio "d" is the average of a switching function "s" over a switching period. If "d" is modulated at a frequency sufficiently lower than the switching frequency, it approximately equals the *low-frequency components* of the *quasi-periodic* switching function "s" at period T_s. Based on the restriction that only one of the two throws of a switch branch can be ON at any instant to prevent the source from short-circuiting for a voltage-fed topology, as depicted by Equations (3.5) and (3.6). The duty-ratios of a switch branch must be

$$d_{r2} = 1 - d_{r1} \qquad \text{for} \quad r = a \sim c \tag{3.26}$$

The state-space equations for the inverter are the 3ϕ voltages v_A, v_B, and v_C and currents i_A, i_B, and i_C which are the six states for the respective capacitor voltages and inductor currents. At any instant, the following equations are always true for the currents through the inductors:

$$(s_{a1} - s_{b1})\, V_{dc} = L\frac{di^*_a}{dt} + v^*_a - L\frac{di^*_b}{dt} - v^*_b \tag{3.27a}$$

$$(s_{b1} - s_{c1})\, V_{dc} = L\frac{di^*_b}{dt} + v^*_b - L\frac{di^*_c}{dt} - v^*_c \tag{3.27b}$$

and

$$(s_{c1} - s_{a1})\, V_{dc} = L\frac{di^*_c}{dt} + v^*_c - L\frac{di^*_a}{dt} - v^*_a \tag{3.27c}$$

where i^*'s and v^*'s are the instantaneous values of currents and voltages for respective inductors and capacitors, to be distinguished from the low-frequency components represented by i's and v's without the asterisks.

By KCL, the currents that flow in and out of a single branch must be equal, thus

$$i^*_a + i^*_b + i^*_c = 0 \tag{3.28}$$

since L_a, L_b, and L_c are the only elements for the current to flow in and out of the source. By substituting

$$i^*_b = -(i^*_c + i^*_a) \tag{3.29}$$

into Equation (3.27a)

$$(s_{a1} - s_{b1})\, V_{dc} = 2L\frac{di^*_a}{dt} + v^*_a - v^*_b + L\frac{di^*_c}{dt} \tag{3.30}$$

rewriting Equation (3.27c) into

$$L\frac{di^*_c}{dt} = (s_{c1} - s_{a1})\, V_{dc} - v^*_c + L\frac{di^*_a}{dt} + v^*_a \tag{3.31}$$

and then combining Equations (3.30) and (3.31), the instantaneous voltage across the inductor L_a can be obtained as

$$L\frac{di^*_a}{dt} = \frac{1}{3}(-2v^*_a + v^*_b + v^*_c) + \frac{1}{3}(2s_{a1} - s_{b1} - s_{c1})\, V_{dc} \tag{3.32a}$$

Similarly, the instantaneous voltages across inductors L_b and L_c can be rewritten as

$$L\frac{di^*_b}{dt} = \frac{1}{3}(v^*_a - 2v^*_b + v^*_c) + \frac{1}{3}(-s_{a1} + 2s_{b1} - s_{c1})\, V_{dc} \tag{3.32b}$$

and

$$L\frac{di^*_c}{dt} = \frac{1}{3}(v^*_a + v^*_b - 2v^*_c) + \frac{1}{3}(s_{a1} - s_{b1} + 2s_{c1})\, V_{dc} \tag{3.32c}$$

respectively.

The instantaneous voltages across the 3ϕ capacitor bank are

$$C\frac{dv^*_a}{dt} = i^*_a - i^*_{R_a} \tag{3.33a}$$

$$C\frac{dv^*_b}{dt} = i^*_b - i^*_{R_b} \tag{3.33b}$$

and

$$C\frac{dv^*_c}{dt} = i^*_c - i^*_{R_b} \tag{3.33c}$$

for phases A, B, and C, respectively. By the superposition theorem, the currents through R_a, R_b, and R_c can be derived as

$$i^*_{R_a} = \frac{1}{3}(2v^*_a - v^*_b - v^*_c) \tag{3.34a}$$

$$i^*_{R_b} = \frac{1}{3}(-v^*_a + 2v^*_b - v^*_c) \tag{3.34b}$$

$$i^*_{R_c} = \frac{1}{3}(-v^*_a - v^*_b + 2v^*_c) \tag{3.34c}$$

Substituting Equation (3.34) into (3.33), the capacitor currents can be rewritten as

$$C\frac{dv^*_a}{dt} = i^*_a - \frac{1}{3}(2v^*_a - v^*_b - v^*_c) \tag{3.35a}$$

$$C\frac{dv^*_b}{dt} = i^*_b - \frac{1}{3}(-v^*_a + 2v^*_b - v^*_c) \tag{3.35b}$$

and

$$C\frac{dv^*_c}{dt} = i^*_c - \frac{1}{3}(-v^*_a - v^*_b + 2v^*_c) \tag{3.35c}$$

for phases A, B, and C at any instance, respectively.

Equations (3.32) and (3.35) are called *switching state-space equations*, which provide exact solutions for all states under any assigned switching scheme. The differential equations for the low-frequency components of the voltages and currents are called *describing equations* [40, 41] which are approximately obtained by replacing the exact current and voltage terms in the switching state-space equations with the corresponding low-frequency terms. For Equations (3.32) and (3.35), this is done by replacing the switching function "s" with the duty-ratio "d" and dropping the asterisks in these equations.

$$L\frac{di_a}{dt} = \frac{1}{3}(-2v_a + v_b + v_c) + \frac{1}{3}(2d_{a1} - d_{b1} - d_{c1})\,V_{dc} \tag{3.36a}$$

$$L\frac{di_b}{dt} = \frac{1}{3}(v_a - 2v_b + v_c) + \frac{1}{3}(-d_{a1} + 2d_{b1} - d_{c1})\,V_{dc} \tag{3.36b}$$

$$L\frac{di_c}{dt} = \frac{1}{3}(v_a + v_b - 2v_c) + \frac{1}{3}(d_{a1} - d_{b1} + 2d_{c1})\,V_{dc} \tag{3.36c}$$

$$C\frac{dv_a}{dt} = i_a - \frac{1}{3R}(2v_a - v_b - v_c) \tag{3.37a}$$

$$C\frac{dv_b}{dt} = i_b - \frac{1}{3R}(-v_a + 2v_b - v_c) \tag{3.37b}$$

$$C\frac{dv_c}{dt} = i_c - \frac{1}{3R}(-v_a - v_b + 2v_c) \tag{3.37c}$$

For 3ϕ voltage-fed inverters, the requirements for the duty ratios are expressed in Equations (3.26) and (3.38)

$$d_{rn} \geq 0 \quad \text{, for } r = a \sim c \text{ and } n = 1 \sim 2 \tag{3.38}$$

If the duty-ratios $d_{a1}/d_{b1}/d_{c1}$ and $d_{a2}/d_{b2}/d_{c2}$ are in the form

$$\begin{aligned} d_{a1} &= \frac{1}{2} + \frac{1}{2} d_m \cos\theta(t) = \frac{1}{2} + \frac{1}{2} d_a \\ d_{b1} &= \frac{1}{2} + \frac{1}{2} d_m \cos\left(\theta(t) - \frac{2\pi}{3} n\right) = \frac{1}{2} + \frac{1}{2} d_b \\ d_{c1} &= \frac{1}{2} + \frac{1}{2} d_m \cos\left(\theta(t) + \frac{2\pi}{3} n\right) = \frac{1}{2} + \frac{1}{2} d_c \end{aligned} \tag{3.39a}$$

$$\begin{aligned} d_{a2} &= \frac{1}{2} - \frac{1}{2} d_m \cos\theta(t) = \frac{1}{2} - \frac{1}{2} d_a \\ d_{b2} &= \frac{1}{2} - \frac{1}{2} d_m \cos\left(\theta(t) - \frac{2\pi}{3} n\right) = \frac{1}{2} - \frac{1}{2} d_b \\ d_{c2} &= \frac{1}{2} - \frac{1}{2} d_m \cos\left(\theta(t) + \frac{2\pi}{3} n\right) = \frac{1}{2} - \frac{1}{2} d_c \end{aligned} \tag{3.39b}$$

where

$$n \in \text{Integer and } n \bmod 3 \neq 0 \tag{3.40}$$

and

$$\begin{aligned} d_m &\leq 1 \\ \theta(t) &= \int_0^t \omega(\tau)\, d\tau \end{aligned} \tag{3.41}$$

Note that Equations (3.39) and (3.41) indicate that the maximum effective modulation amplitude is $d_m/2$ for the sinusoidal PWM. For a voltage-fed inverter, the output voltage is directly proportional to the effective modulation amplitude. This amplitude can be increased to $d_m/\sqrt{3}$ by employing the six-stepped PWM [43]. Therefore, the maximum output voltage can be in creased by the factor of $2/\sqrt{3}$ compared with the sinusoidal PWM.

Equations (3.36) and (3.37) can be put into a state-space matrix form with six states and one input

$$\mathbf{P}\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{3.42}$$

where **x** denotes the state vector and is composed of the inductor currents and the capacitor voltages. The vector **u** denotes the input which is the source voltage V_{dc}. **A**, **B**, and **P** are the coefficient matrices:

$$\mathbf{x} = \left[i_a\ i_b\ i_c\ v_a\ v_b\ v_c\right]^T \tag{3.43a}$$

$$\mathbf{u} = V_{dc} \tag{3.43b}$$

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & 0 & 0 & \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \\ 1 & 0 & 0 & -\frac{2}{3R} & \frac{1}{3R} & \frac{1}{3R} \\ 0 & 1 & 0 & \frac{1}{3R} & -\frac{2}{3R} & \frac{1}{3R} \\ 0 & 0 & 1 & \frac{1}{3R} & \frac{1}{3R} & -\frac{2}{3R} \end{bmatrix} \tag{3.43c}$$

$$\mathbf{B} = \frac{1}{2}\begin{bmatrix} d_m\cos\theta(t) \\ d_m\cos\left(\theta(t) - \frac{2\pi}{3}n\right) \\ d_m\cos\left(\theta(t) + \frac{2\pi}{3}n\right) \\ 0 \\ 0 \\ 0 \end{bmatrix}, \qquad \mathbf{P} = \begin{bmatrix} L & 0 & 0 & 0 & 0 & 0 \\ 0 & L & 0 & 0 & 0 & 0 \\ 0 & 0 & L & 0 & 0 & 0 \\ 0 & 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & 0 & C \end{bmatrix} \tag{3.43d,e}$$

With the duty ratios assigned in the form of Equation (3.39), the steady-state low-frequency output voltages are balanced 3ϕ sinusoidal [41]. A PSpice® simulation for the PWM inverter, with duty ratios in the form of Equation (3.39) and controlled by UPWM mode, has been done. The waveforms are shown in Figure 3.16 with all parameters listed. From the figure, it is clearly seen that the output voltage is a replica of the AC part of the duty-ratio with only its phase shifted.

The steady-state averaging and small-signal dynamic analysis can be done by performing the *d-q* or *o-f-b* transformation on Equations (3.42) and (3.43) as done in the analysis of 3ϕ power systems [41, 43, 56 - 54]. The two equations are also the bases for other PWM modelling techniques [63] of 3ϕ voltage-fed inverters.

For a voltage-fed active filter, Equations (3.36) and (3.37) work in the way as discussed in Section 3.1 for HPWM operations. When the inverter acts as a stand-alone power supply, there is no phase-synchronization problem since the inverter is not required to synchronize with another system whose phase is the reference. Hence, the phase angle in the duty ratio is not important as long as only balanced three-phase voltages are desired. However, in the cases of parallel operation with other power supplies or in active filtering, the relative phase of the inverter-generated voltage along with its amplitude are both required for success of operation. Suppose that the PWM inverter switched at a frequency f_s is required to provide balanced 3ϕ output voltages at a frequency f_o, with a phase shift φ referred to some other source, as

$$\begin{aligned} v_a &= V_m \sin(\omega_o t + \varphi) \\ v_b &= V_m \sin\left(\omega_o t + \varphi - \frac{2\pi}{3}\right) \\ v_c &= V_m \sin\left(\omega_o t + \varphi + \frac{2\pi}{3}\right) \end{aligned} \tag{3.44}$$

where ω_o is the angular frequency of the output, $\omega_o = 2\pi f_0$, and $f_o \ll f_s$. Since it is a balanced 3ϕ output,

$$\sum_{r=a}^{c} v_r = 0 \tag{3.45}$$

and the duty-ratios must be in the form of balanced three-phase, it can be shown that phase currents and voltages are decoupled and only the current and voltage of one phase are sufficient to determine the low-frequency duty-ratio for the required output. By rewriting Equations (3.36a) and (3.37a) into

$$\begin{aligned} L\frac{di_a}{dt} &= \frac{1}{3}(-2v_a + v_b + v_c) + \frac{1}{3}(2d_{a1} - d_{b1} - d_{c1})V_{dc} \\ &= -v_a + \frac{1}{3}(v_a + v_b + v_c) + \frac{d_a}{2}V_{dc} - \frac{1}{3}\left(\frac{d_a}{2} + \frac{d_b}{2} + \frac{d_c}{2}\right)V_{dc} \\ &= -v_a + \frac{d_a}{2}V_{dc} \end{aligned} \tag{3.46}$$

$$\begin{aligned} C\frac{dv_a}{dt} &= i_a - \frac{1}{3R}(2v_a - v_b - v_c) \\ &= i_a - \frac{v_a}{R} + \frac{1}{3R}(v_a + v_b + v_c) \\ &= i_a - \frac{v_a}{R} \end{aligned} \tag{3.47}$$

it can be seen that Equations (3.46) and (3.47) resemble Equations (3.17) and (3.18). The d_a, d_b, and d_c in the above two equations are the AC components in the duty ratios d_{a1}/d_{a2}, d_{b1}/d_{b2}, and d_{c1}/d_{c2} as derived in Equation (3.39), respectively. The DC parts of the duty ratios sum up to zero and have no effect in determining d_a, d_b, and d_c. The low-frequency d_a can be found in the same way as Equation (3.20) by substituting Equation (3.47) into (3.46),

$$d_a(t) = \sqrt{\left[1-\left(\frac{\omega_o}{\omega_c}\right)^2\right]^2+\left(\frac{1}{Q}\frac{\omega_o}{\omega_c}\right)^2} * \frac{2V_m}{V_{dc}}\sin\left(\omega_o t+\varphi+\tan^{-1}\frac{(1/Q)\ (\omega_o/\omega_c)}{1-(\omega_o/\omega_c)^2}\right), \quad |d_a| \le 1 \tag{3.48}$$

for linear modulation, where ω_c and Q have the same definitions as in Equation (3.21) for the case of 1ϕ inverter.

Note that there is a factor of 2 difference between Equation (3.20) for the 1ϕ case and Equation (3.48) for the 3ϕ case, due to the fact that the voltage by Equation (3.20) in 1ϕ inverter is the line-to-line voltage but the voltage by Equation (3.48) is the phase-to-neutral voltage of 3ϕ Y-Y connection. Hence, in sinusoidal PWM where m_a is always less than one, the theoretic maximal peak amplitude of line-to-line output voltage is equal to the amplitude of supply voltage V_{dc} for a 1ϕ inverter and is equal to $\sqrt{3}\,V_{dc}/2$ for a 3ϕ inverter. Since the output voltage amplitude of a voltage-fed inverter is always smaller than the amplitude of input voltage, voltage-fed inverters are classified as "buck" inverters as the buck converters in DC/DC conversion [3, 4, 64]. However, by employing the six-stepped PWM [43], the 3ϕ inverter can have the maximum line-to-line voltage of V_{dc} instead of $\sqrt{3}\,V_{dc}/2$ because the effective modulation amplitude in Equation (3.39) is $d_m/\sqrt{3}$ instead of $d_m/2$.

With d_a defined by Equation (3.48), the actual duty-ratios associated with the switching functions s_{11} and s_{22} can be assigned as

$$d_{a1} = \frac{1}{2} + \frac{1}{2}d_a(t)$$
$$d_{a2} = \frac{1}{2} - \frac{1}{2}d_a(t) \tag{2.49}$$

and the corresponding duty-ratios for the switching functions of phases B and C are defined in the same way.

3.4. Operations of Three-Phase Current-Fed Inverter

A 3ϕ current-fed inverter with power MOSFETs as the switches is shown in Figure 3.17. As in the voltage-fed inverter, the output capacitor and load of each phase are assumed balanced and are in Y-Y connection. The diodes in series with the MOSFETs are used to block the negative part of the AC output voltage since the power MOSFETs (BJTs, IGBTs) do not possess the full reverse voltage blocking ability. If other semiconductor devices capable of blocking reverse voltages, such as thyristors for very high power application, are employed, the reverse-blocking diode can be omitted. The diode and MOSFET on the DC side are employed to act as a buck DC/DC converter to adjust the average DC voltage, hence the current, supplied to the inverter. They can be modeled as a 1P2T switch with the pole labeled as Z in the figure.

The current-fed inverter, as redrawn in Figure 3.18 with all inverter MOSFETs and diodes replaced by one 1P2T and two 1P3T switch branches, can be analyzed by the state-space method in the same way as the voltage-fed inverter in Section 3.3 under the same assumptions [40, 41]. The relationship between corresponding $s_{1a}/s_{1b}/s_{1c}$ and $s_{2a}/s_{2b}/s_{2c}$ and $d_{1a}/d_{ib}/d_{1c}$ and $d_{2a}/d_{2b}/d_{2c}$ can be illustrated in Figure 3.19. The duty-ratios for the three throws associated with the same pole must be

$$d_{na} + d_{nb} + d_{nc} = 1, \quad \text{for } n = 1 \text{ or } 2 \tag{3.50}$$

The state-space equations for the current-fed inverter are composed of the phase voltages v_A, v_B, and v_C of the output capacitors and the inductor current i_{dc}. The current-fed inverter is a fourth-order system in contrast with the sixth-order system of a voltage-fed inverter.

From Figure 3.19, the instantaneous voltage across the inductor can be written as

$$\begin{aligned} L\frac{di^*_L}{dt} &= v^*_{ZX} = v^*_{ZN} - \left(v^*_{XG} - v^*_{NG}\right) \\ &= s^*_d V_{dc} - [(s_{1a} - s_{2a})v^*_a + (s_{1b} - s_{2b})v^*_b + (s_{1c} - s_{2c})v^*_c] \end{aligned} \tag{3.51}$$

and the instantaneous currents through the output capacitor bank can be written as

$$\begin{aligned} C\frac{dv^*_a}{dt} &= (s_{1a} - s_{2a})i^*_L - i^*_{R_a} \\ &= (s_{1a} - s_{2a})i^*_L - \frac{1}{3}(2v^*_a - v^*_b - v^*_c) \end{aligned} \tag{3.52a}$$

$$\begin{aligned} C\frac{dv^*_b}{dt} &= (s_{1b} - s_{2b})i^*_L - i^*_{R_b} \\ &= (s_{1b} - s_{2b})i^*_L - \frac{1}{3}(-v^*_a + 2v^*_b - v^*_c) \end{aligned} \tag{3.52b}$$

and

$$\begin{aligned} C\frac{dv^*_c}{dt} &= (s_{1c} - s_{2c})i^*_L - i^*_{R_c} \\ &= (s_{1a} - s_{2a})i^*_L - \frac{1}{3}(-v^*_a - v^*_b + 2v^*_c) \end{aligned} \tag{3.52c}$$

with the phase load currents expressed in Equation (3.34).

As in the case of Section 3.3, the above switching state-space equations give the exact solutions for the states under any given eligible switching scheme. The describing equations that depict the low-frequency behavior of the PWM inverter are obtained by

replacing the switching functions with the respective duty-ratios and dropping the asterisks in the above equations

$$L\frac{di_L}{dt} = d_d V_{dc} - [(d_{1a} - d_{2a})v_a + (d_{1b} - d_{2b})v_b + (d_{1c} - d_{2c})v_c] \tag{3.53}$$

$$C\frac{dv_a}{dt} = (d_{1a} - d_{2a})i_L - \frac{1}{3R}(2v_a - v_b - v_c) \tag{3.54a}$$

$$C\frac{dv_b}{dt} = (d_{2b} - d_{2c})i_L - \frac{1}{3R}(-v_a + 2v_b - v_c) \tag{3.54b}$$

$$C\frac{dv_c}{dt} = (d_{1c} - d_{2c})i_L - \frac{1}{3R}(-v_a - v_b + 2v_c) \tag{3.54c}$$

By defining the effective duty-ratio as

$$d_r = d_{1r} - d_{2r}, \quad r = a \sim c \tag{3.55}$$

the fourth-order state-space system can be put into the matrix form as

$$\mathbf{P}\frac{d\mathbf{x}}{dt} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{3.56}$$

where

$$\mathbf{x} = \begin{bmatrix} i_L & v_a & v_b & v_c \end{bmatrix}^T \tag{3.57a}$$

$$\mathbf{u} = V_{dc} \tag{3.57b}$$

$$\mathbf{A} = \begin{bmatrix} 0 & -d_a & -d_b & -d_c \\ d_a & -\frac{2}{3R} & \frac{1}{3R} & \frac{1}{3R} \\ d_b & \frac{1}{3R} & -\frac{2}{3R} & \frac{1}{3R} \\ d_c & \frac{1}{3R} & \frac{1}{3R} & -\frac{2}{3R} \end{bmatrix} \tag{3.57c}$$

$$\mathbf{B} = \begin{bmatrix} d_d \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{P} = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & C & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C \end{bmatrix} \tag{3.57d,e}$$

It has been derived [41] that if

(1) the effective duty-ratios for the 3ϕ inverter are balanced in the forms of

$$\begin{aligned} d_a &= \frac{2}{3} d_m \sin\theta(t) \\ d_b &= \frac{2}{3} d_m \sin\left(\theta(t) - \frac{2\pi}{3} n\right) \\ d_c &= \frac{2}{3} d_m \sin\left(\theta(t) + \frac{2\pi}{3} n\right) \end{aligned} \tag{3.58}$$

where n is defined in Equation (3.40) and d_m and $\theta(t)$ are defined in Equation (3.41), and

(2) the duty-ratios for the two throws, which are from different branches but connected to the same phase, are defined as

$$\begin{aligned} d_{1r} &= \frac{1}{3} + \frac{1}{2} d_r \\ d_{2r} &= \frac{1}{3} - \frac{1}{2} d_r \end{aligned} . \tag{3.59}$$

The output voltages v_a, v_b, and v_c will be balanced sinusoidal, too. Figure 3.20 shows the waveforms of a current-fed inverter simulated in PSpice® with duty-ratios in the forms of Equations (3.58) and (3.59). Because the current-fed topology does not possess intrinsic low-pass filters as the voltage-fed does, the ripples of switching frequency appear on the voltage v_a across the output capacitor as shown in Figure 3.20(b). However, this is not an obstacle for the current-fed applications since an optional extra low-pass filter can be added to the capacitor bank to remove the switching ripples as shown in Figure 3.20(c). From the figure, it is clearly seen that the output voltage amplitude is higher than the

amplitude of input voltage. Hence, current-fed inverters are equivalent to the "boost" converter in DC/DC conversion [3, 4, 64].

As mentioned in Section 3.3, the steady-state averaging and small-signal dynamic analyses of the current-fed inverter can be performed after the *d-q* or *o-f-b* transformation are applied to Equations (3.56) and (3.57) as done in the analysis of 3ϕ power systems [41, 43, 54 - 56].

Similar to the voltage-fed inverter, balanced 3ϕ voltages as shown in Equation (3.44) can be obtained from the current-fed inverter by rewriting Equation (3.54) as

$$\begin{aligned} C\frac{dv_a}{dt} &= (d_{1a} - d_{2a})\, i_L - \frac{1}{3R}(2v_a - v_b - v_c) \\ &= d_a i_L - \frac{v_a}{R} \end{aligned} \tag{3.60}$$

Rearranging Equation (3.60) by putting $d_a i_L$ on the left-hand side of the equation yields

$$\begin{aligned} d_a i_L &= C\frac{dv_a}{dt} + \frac{v_a}{R} \\ &= (\omega_o C)\, V_m \cos(\omega_o t + \varphi) + \frac{V_m}{R}\sin(\omega_o t + \varphi) \\ &= \sqrt{(\omega_o C)^2 + \frac{1}{R^2}}\, V_m \sin\left(\omega_o t + \varphi + \tan^{-1}\omega_o CR\right) \end{aligned} \tag{3.61}$$

With the v_a known and the restriction on the magnitude of d_a described in Equations (3.41) and (3.58), the required minimum DC current $I_{L_{min}}$ for the inverter to work is obtained by the requirement

$$|d_a| = \left| \frac{\sqrt{(\omega_o C)^2 + \frac{1}{R^2}}\, V_m}{I_{L_{min}}} \right| \le \frac{2}{3} \tag{3.62}$$

$$\therefore I_{L_{min}} \geq \frac{3}{2}\left|\sqrt{(\omega_o C)^2 + \frac{1}{R^2}}V_m\right| \tag{3.63}$$

$$|d_a| = \frac{1}{I_{L_{min}}}\left(\sqrt{(\omega_o C)^2 + \frac{1}{R^2}}V_m\right) \tag{3.64}$$

Since the inductor current i_L is approximately DC, by substituting Equations (3.44) and (3.64) into Equation (3.53), the required duty-ratio d_d for V_{dc} can be obtained as

$$\begin{aligned} L\frac{di_L}{dt} &= d_d V_{dc} - [(d_{1a} - d_{2a})v_a + (d_{1b} - d_{2b})v_b + (d_{1c} - d_{2c})v_c] \\ &= d_d V_{dc} - [d_a v_a + d_b v_b + d_c v_c] \\ &= d_d V_{dc} - \frac{1}{I_{L_{min}}}\left[\left(C\frac{dv_a}{dt} + \frac{v_a}{R}\right)v_a + \left(C\frac{dv_b}{dt} + \frac{v_b}{R}\right)v_b + \left(C\frac{dv_c}{dt} + \frac{v_c}{R}\right)v_c\right] \\ &= d_d V_{dc} - \frac{1}{I_{L_{min}}}\sqrt{(\omega_o C)^2 + \frac{1}{R^2}}V_m^2\left[\frac{3}{2}\cos\left(\tan^{-1}\omega_o CR\right)\right] \end{aligned} \tag{3.65}$$

With basic trigonometric rule, the above equation can be simplified as

$$L\frac{di_L}{dt} = d_d V_{dc} - \frac{1}{I_{L_{min}}}\left(\frac{3}{2}\frac{V_m^2}{R}\right) \tag{3.66}$$

By equating the left-hand side of Equation (3.66) to zero, the averaged voltage for the inverter to work is

$$d_d V_{dc} = \frac{3}{2}\frac{1}{I_{L_{min}}}\frac{V_m^2}{R} \tag{3.67}$$

that is, the input power equals the output power if the term $I_{L_{min}}$ moves to the left-hand side. Note that the coefficient 3/2 in the minimum required current $I_{L_{min}}$ in Equation (3.63) can be reduced to 1 if the six-stepped PWM [43] is employed.

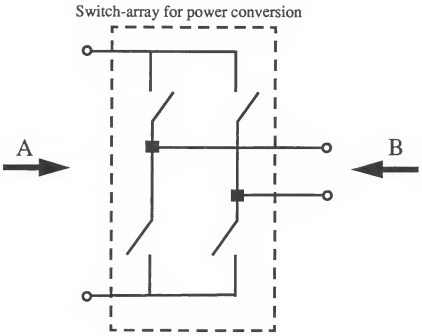
Equations (3.63) to (3.67) are only for the steady-state values of input voltage, current, and respective duty ratios for the switches under the assumption that the outputs are well-balanced 3ϕ voltages. However, the small-signal dynamic analysis performed after the change of reference frame [41, 43, 54 - 56] is indispensable for selections of the L, C, and the control loop compensation to assure inverter stability in feedback control.

Table 3-1: Nomenclature for PWM methods.

$\overline{?}$	$\overline{x}$ is the low-frequency components of x.
BPWM	Bipolar PWM
c	PWM carrier waveform or signal
C	Filter capacitor
d_e	Effective duty ratio, $-1 < d_e < 1$ for linear modulation
f_o	Output frequency; modulation frequency
f_s	Switching frequency; carrier frequency
HPWM	Hybrid PWM
h_{HPWM}	HPWM harmonic order
i_L	Inductor current
k	Integer for locating sideband groups
l	Integer for locating sidebands
m	Modulation waveform or signal
m_a	Amplitude modulation ratio
m_f	Frequency modulation ratio
m'_f	Effective frequency modulation ratio
Q	Quality factor
R	Load resistance
S_{11}	Switch (also: S_{12}, S_{21}, and S_{22})
s_{11}	Switching function of S_{11} (also: s_{12}, s_{21}, and s_{22})
UPWM	Unipolar PWM
v_A, v_B	Voltages at nodes A and B
v_{AB}	Bridge output voltage
V_{dc}	Dc input voltage
$V_{h_{HPWM}}$	Amplitude of harmonic order h_{HPWM}

Table 3-1: continued.

V_m	Amplitude of output voltage
v_o	Output voltage
ω_c	LC corner frequency
ω_o	Output angular frequency



Output \ Input	DC	AC
DC	Converter	Rectifier
AC	Inverter	/

Figure 3.1. The basic constituents and classification of power converters.

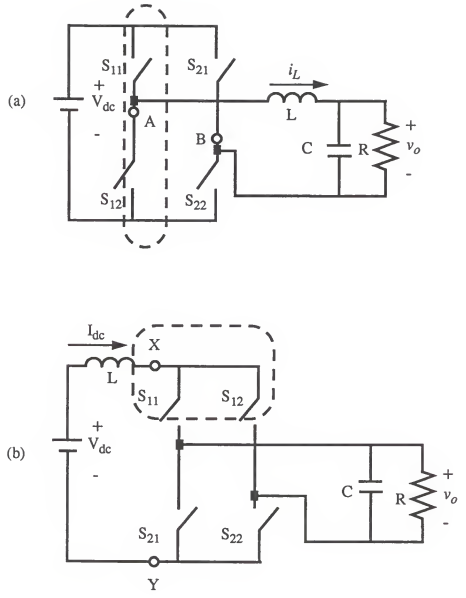


Figure 3.2. The single-phase voltage-fed inverter (a) and current-fed inverter (b).

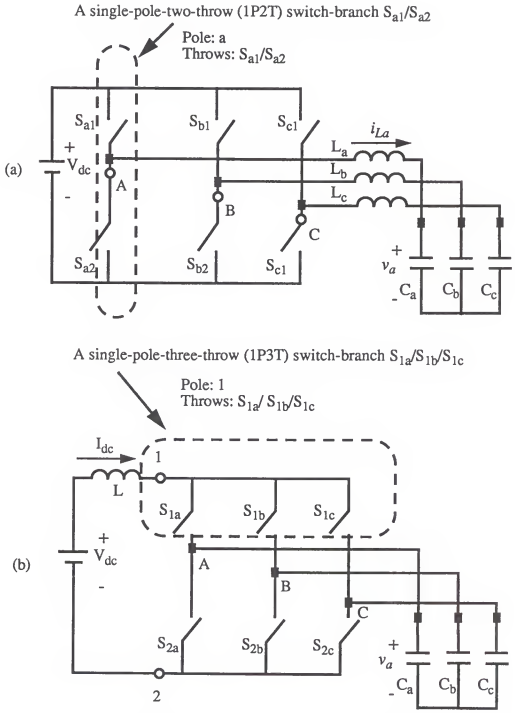


Figure 3.3. The three-phase voltage-fed inverter (a) and current-fed inverter (b).

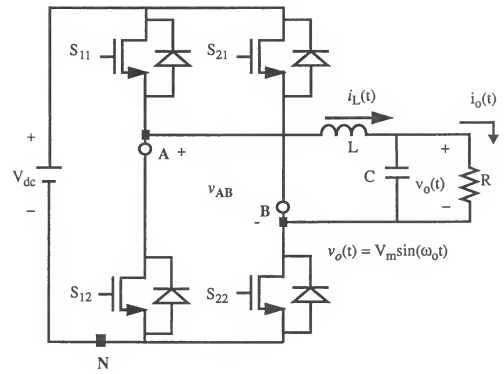


Figure 3.4. The full-bridge inverter with power MOSFETs as switch throws.

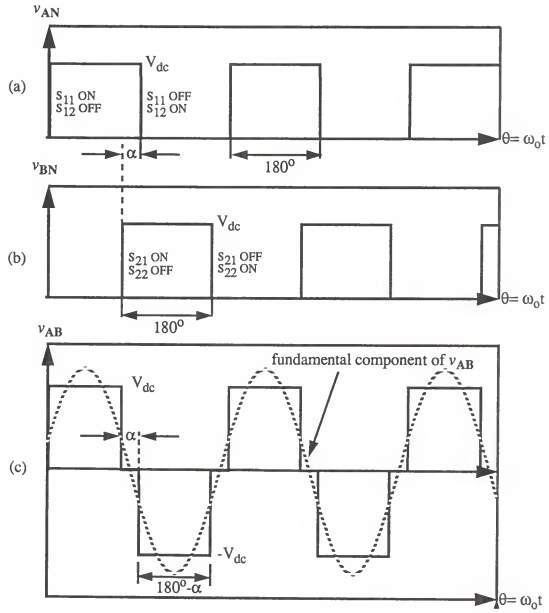


Figure 3.5. The output voltage waveforms of the full-bridge inverter in Figure 3.4 employing the phase-shifted square-wave drives.
(a) The voltage at the pole A;
(b) The voltage at the pole B;
(c) The output voltage v_{AB}.

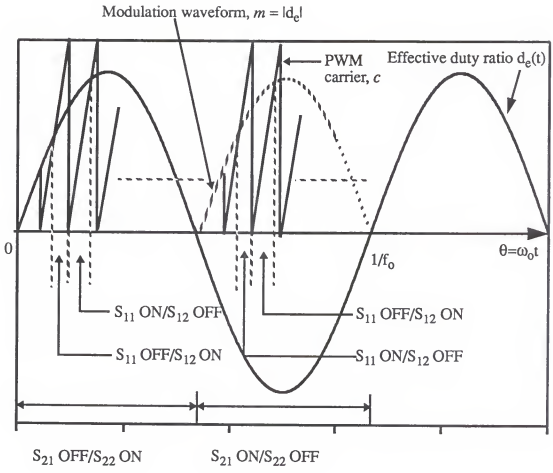


Figure 3.6. The HPWM switching operations of the full-bridge inverter in Figure 3.4.

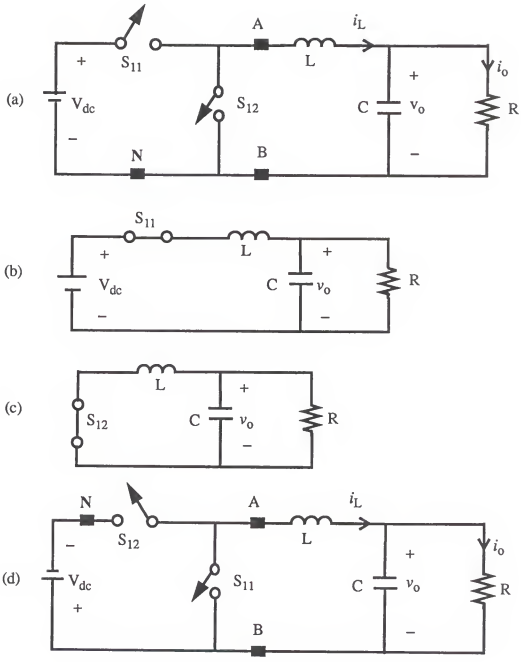


Figure 3.7. Positive buck converter (a) and its switched circuits (b) and (c); Negative buck converter (d).

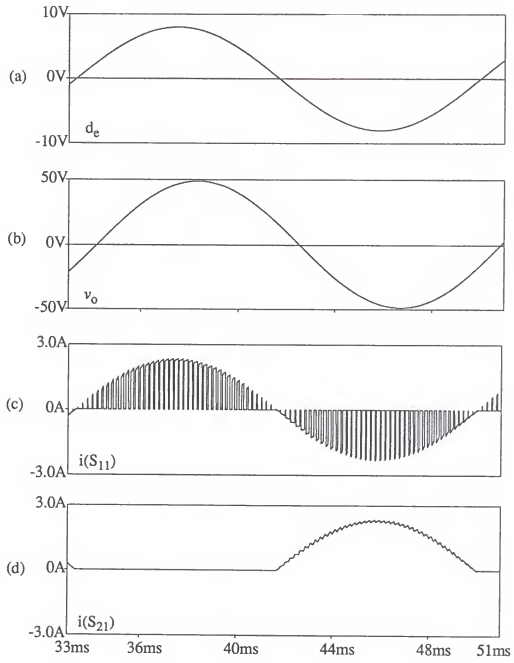


Figure 3.8. Simulated HPWM waveforms for d_e (a), v_o (b), and the currents through S_{11} (c) and S_{21} (d)

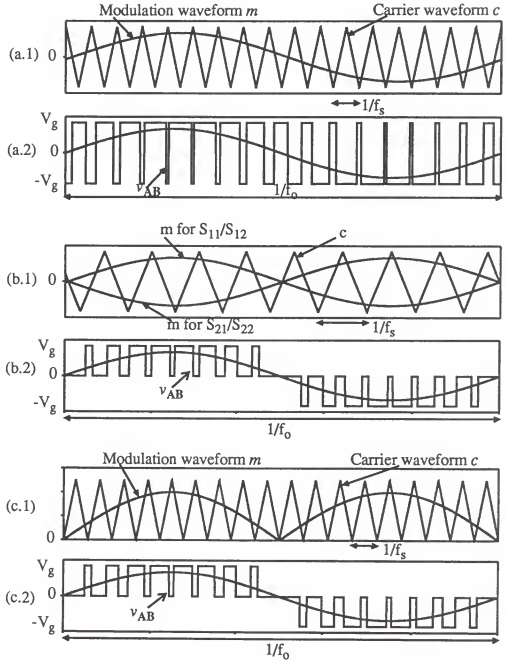


Figure 3.9. Modulation and carrier waveforms (1) and v_{AB} (2) for
(a) BPWM with m_a= 0.8 and m_f= 17;
(b) UPWM with m_a= 0.8 and m_f= 9;
(c) HPWM with m_a= 0.8 and m_f= 18.

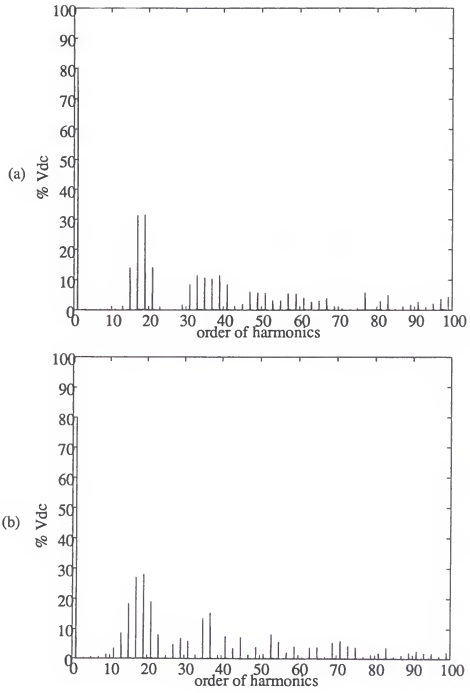


Figure 3.10. Harmonic spectra of v_{AB} generated using a triangular carrier.
(a) HPWM with m_a= 0.8 and m_f= 18;
(b) UPWM with m_a= 0.8 and m_f= 9.

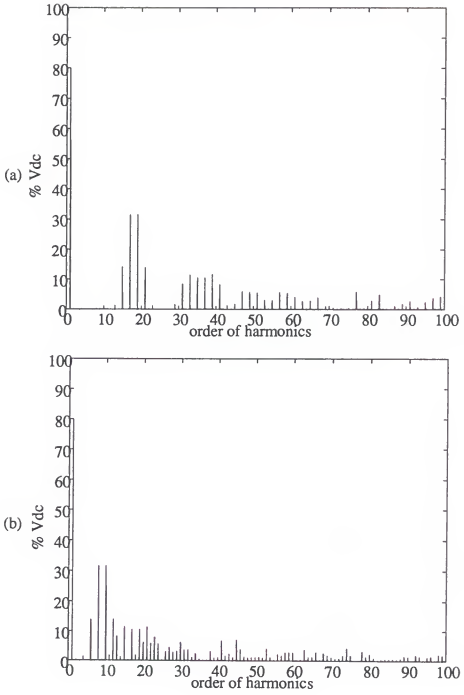


Figure 3.11. Harmonic spectra of v_{AB} generated using a ramp carrier.
(a) HPWM with m_a= 0.8 and m_f= 18;
(b) UPWM with m_a= 0.8 and m_f= 9.

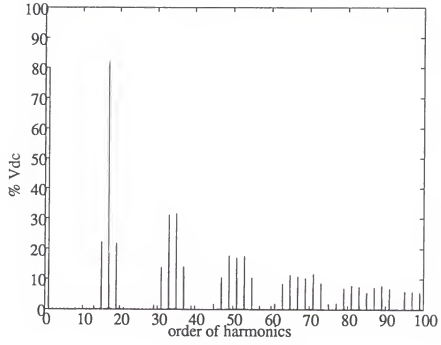


Figure 3.12. Harmonic spectrum of v_{AB} generated using a triangular carrier for BPWM with m_a=0.8 and m_f=17.

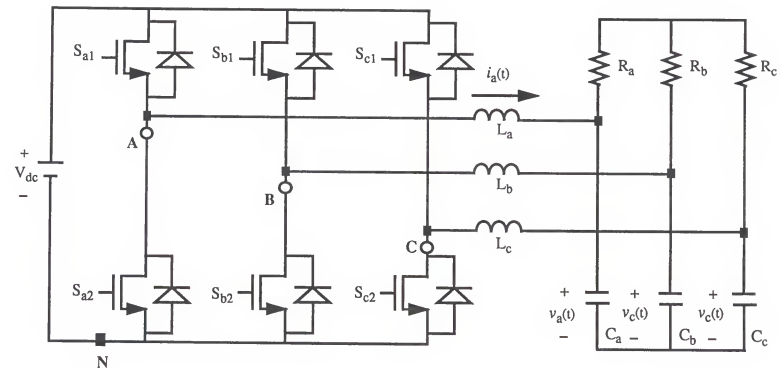


Figure 3.13. A 3ϕ voltage-fed inverter with Y-Y connection of capacitor bank and load.

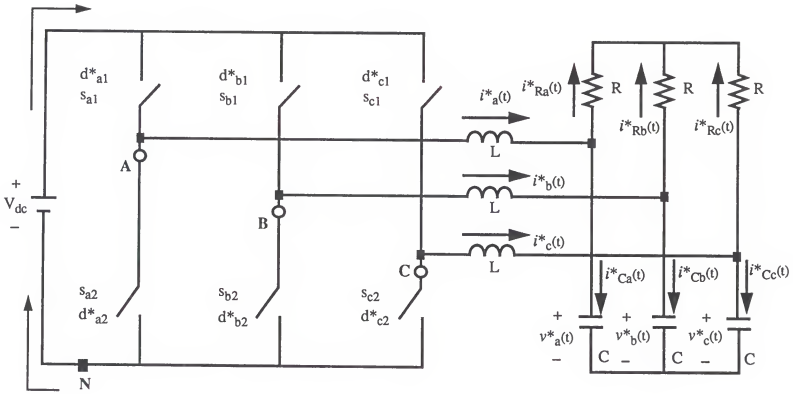


Figure 3.14. Three-phase voltage-fed inverter with one-pole-two-throw switch model.

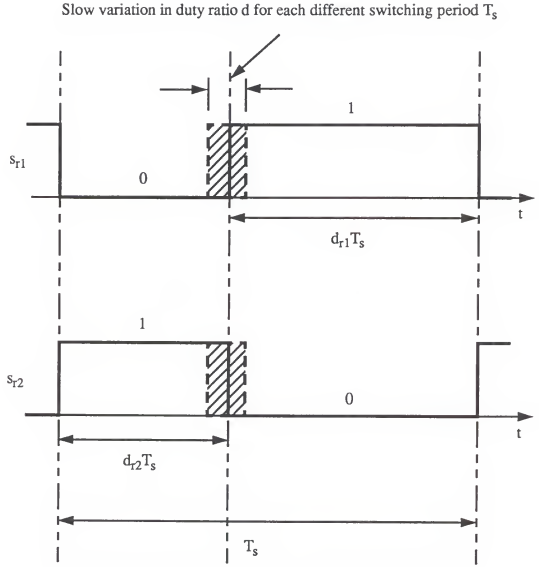
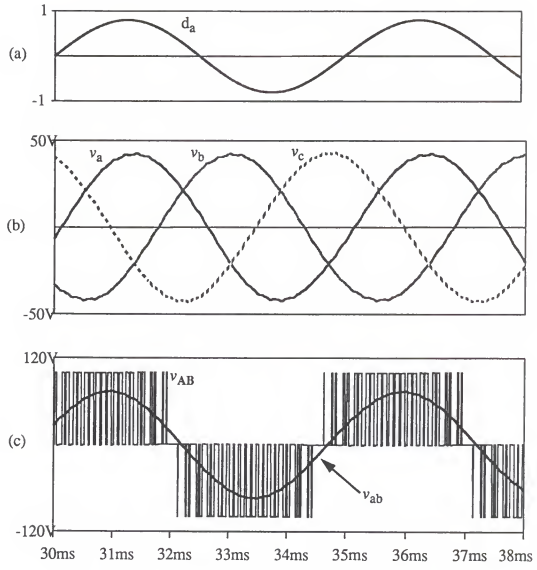


Figure 3.15. Switching functions s_{r1}/s_{r2} and duty-ratios d_{r1}/d_{r2} in a switch branch r.



Simulation parameters			
V_{dc}= 100V	d_m= 0.8	f_o= 200Hz	f_s= 5kHz
L= 1mH	C= 50μF	R= 10Ω	UPWM

Figure 3.16. Simulated waveforms of a 3ϕ voltage-fed inverter.
(a) Duty-ratio d_a;
(b) Phase voltages v_a, v_b, and v_c;
(c) Unfiltered (v_{AB}) and filtered (v_{ab}) line-to-line voltages.

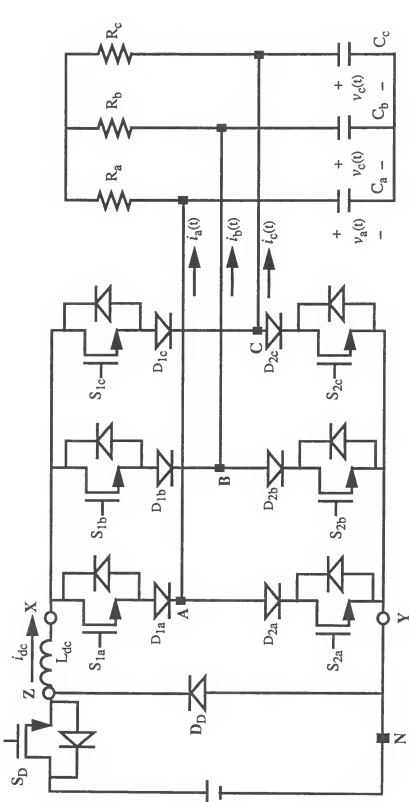


Figure 3.17. A 3ϕ current-fed inverter with Y-Y connection of capacitor bank and load.

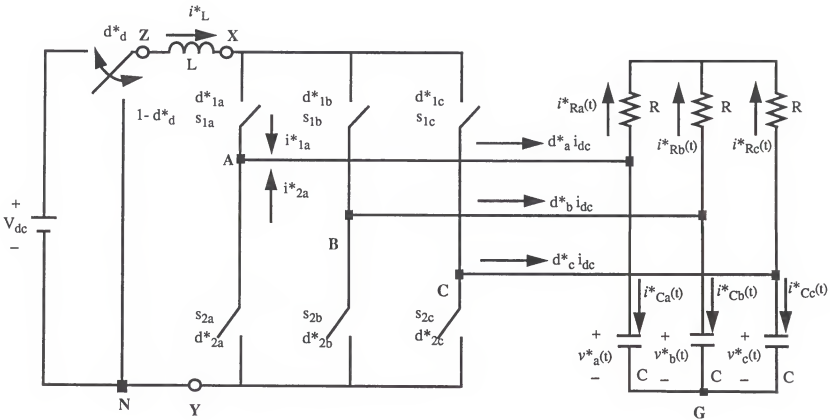
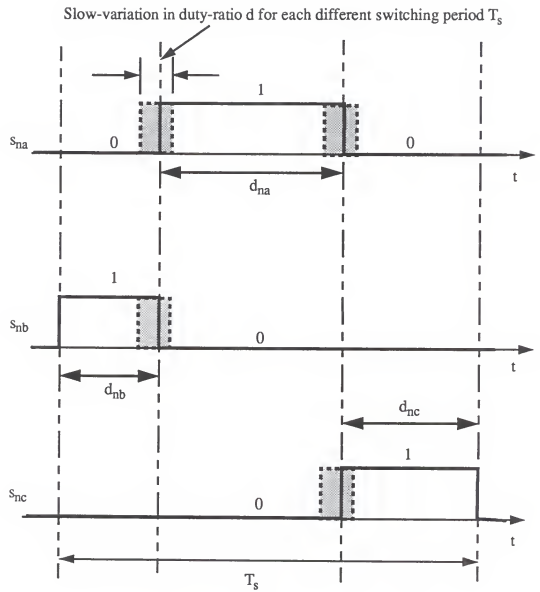
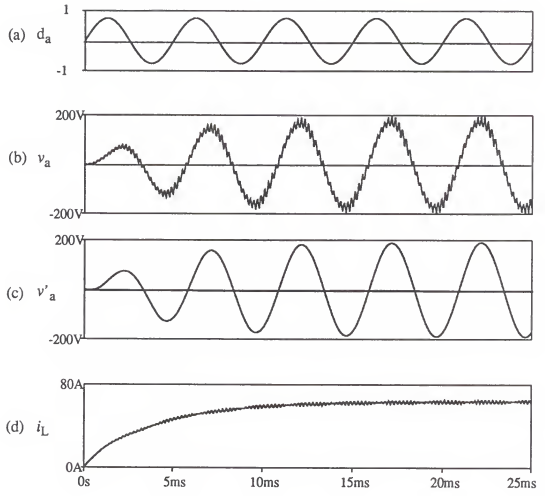


Figure 3.18. Three-phase current-fed inverter with one-pole-three-throw switches for the ac power conversion circuitry.



n=1 and 2 for poles **X** and **Y**, respectively, in a 3ϕ current-fed inverter

Figure 3.19. Switching functions $s_{na}/s_{nb}/s_{nc}$ and duty-ratios $d_{na}/d_{nb}/d_{nc}$ in a switch branch n.



Simulation parameters			
V_{dc}= 100V	d_m= 0.9	f_o= 200Hz	f_s= 5kHz
L= 5mH	C= 150μF	R= 10Ω	UPWM

Figure 3.20. Simulated waveforms of a 3ϕ current-fed inverter.
(a) Duty-ratio d_a;
(b) Voltage across phase-A output capacitor v_a;
(c) Load voltage v'_a (v_a through a LC low-pass filter);
(d) Inductor current i_L.

CHAPTER 4
THE PROPOSED LOW-RATINGS POWER QUALITY SOLUTION

As discussed in Section 2.2, an active filter in series with a passive filter is well-suited for the elimination of source current and load voltage harmonics. The disadvantage of this filter combination is that, for the conventional series resonant passive filters tuned at harmonic frequencies, there is phase-leading fundamental current through the circuitry of the active filter, which increases the power and component ratings of the active filter (inverter).

To avoid a significant amount of fundamental current passing through the inverter when power factor correction is not required, this dissertation proposes an LC parallel resonant filter tuned at the fundamental frequency as shown in Figure 4.1 to replace the conventional passive filter, consisting of three parallel LC series resonant filters tuned at the 5th, 7th, and 11th harmonics. The proposed hybrid parallel LC passive/active filter configurations are shown in Figures 4.2 and 4.3, with a current-fed inverter and a voltage-fed inverter as the active filter, respectively.

The operational principles of the current-fed and voltage-fed inverters as active filters in the power system and the describing state-space equations [41] are presented in Sections 4.1 and 4.2, respectively. To justify the low-rating claim of this study, the loss mechanism of the current-fed hybrid filter and comparison of the losses between the proposed and the conventional active/passive filter are presented in Section 4.3. An experiment based on the analysis of the current-fed active filter done in this chapter will be

presented in the next chapter.

4.1. A Current-Fed Inverter as the Active Filter

To explain the operations of the current-fed active filter clearly, Figure 4.2 is schematically redrawn in Figure 4.4 with only phase A of the inverter shown and all the subscripts "$_a$"s denoting the phase A for the power system are omitted to simplify the variable notations. The *single-pole-double-throw* switch on the DC side is used to adjust the average input voltage v_{dc} only and is removed for simplicity. The derivations of the switching state-space equations for the active filter is the same as that described in Section 3.3 for the inverter; those steps are not repeated here.

Since the phases of a balanced 3ϕ system are decoupled for both the inverter and active filter, and the analysis done on one phase is directly applicable to other phases, only the equations for phase A are presented. Using the procedures in Section 3.3, the describing equations [41, 43] for the active filter and the system can be derived as follows.

In order to synthesize a voltage that is the negative of the sum of the harmonic voltages across the passive filter, the duty-ratio of the inverter must in the form

$$\begin{aligned} d_a i_{dc} &= -i_p + C_i \cdot \frac{d}{dt}\left(\sum_{h\neq 1} v_{ih}\right) \\ &= -\left(i_{pf} + \sum_{h\neq 1} i_{ph}\right) + C_i \cdot \frac{d}{dt}\left(\sum_{h\neq 1} -v_{ph}\right) \\ &= -i_{pf} - \sum_{h\neq 1} i_{ph} - \sum_{h\neq 1} C_i \cdot \frac{dv_{ph}}{dt} \end{aligned} \tag{4.1}$$

For the terms on the right-hand side of Equation (4.1):

(1) i_{pf} is the fundamental current through the passive filter caused by mismatched L_p, C_p and the parasitic resistances of the filter,

(2) i_{ph} is a harmonic current of the h-th order

$$\begin{aligned} i_{pf} &= i_{L_p f} + i_{C_p f} \\ i_{ph} &= i_{L_p h} + i_{C_p h} \quad \text{for every h'} \end{aligned} \tag{4.2}$$

(3) v_{ph} is the voltage drop across the passive filter by i_{ph}, and

(4) v_{ih} is the voltage generated by the active filter which is required to be equal to $-v_{ph}$.

where C_i is the output capacitor of the inverter. Based on the assumptions that v_{Lf} and $\Sigma_h i_{Lh}$ are known or can be measured, each of the terms in Equation (4.1) can be calculated and the required duty ratio d_a for harmonic elimination can be obtained. Note that all variables for voltages and currents are distinguished by the last subscripts "$_f$" and "$_h$" for the fundamental and harmonic terms, respectively.

The individual current and voltage of the parallelled L_p and C_p can be written as

$$\begin{aligned} i_{C_p f} &= C_p \cdot \frac{d}{dt}\left(v_{pf} - R_{C_p} \cdot i_{C_p f} \right) \\ C_p \cdot \frac{dv_{pf}}{dt} &= \left(1 + C_p R_{C_p} \cdot \frac{d}{dt} \right) i_{C_p f} \end{aligned} \tag{4.3}$$

for the fundamental current and

$$\begin{aligned} \sum_{h \neq 1} i_{C_p h} &= C_p \cdot \frac{d}{dt}\left(\sum_{h \neq 1} v_{ph} - R_{C_p} \cdot \sum_{h \neq 1} i_{C_p h} \right) \\ \sum_{h \neq 1} C_p \cdot \frac{dv_{ph}}{dt} &= \sum_{h \neq 1} \left(1 + C_p R_{C_p} \cdot \frac{d}{dt} \right) i_{C_p h} \end{aligned} \tag{4.4}$$

for the harmonic current through the capacitor of the passive filter. The equations for the passive filter inductor are

$$
\begin{aligned}
v_{pf} &= L_p \cdot \frac{d}{dt} i_{L_p f} + R_{L_p} \cdot i_{L_p f} \\
\sum_{h \neq 1} v_{ph} &= \sum_{h \neq 1} \left(R_{L_p} + L_p \cdot \frac{d}{dt} \right) i_{L_p h}
\end{aligned}
\tag{4.5}
$$

where L_p and C_p are tuned at the fundamental frequency ω_o

$$
\omega_o = \frac{1}{\sqrt{L_p C_p}} \tag{4.6}
$$

R_{C_p} is the effective series resistance (ESR) of the capacitor C_p, and R_{L_p} is the series resistance associated with the filter inductor L_p. The only adequate way to determine R_{C_p} and R_{L_p} are by measurement. The quality factors for C_p and L_p indicating the parasitic resistances can be determines as

$$
\begin{aligned}
Q_{C_p} &= \frac{1}{\omega_o C_p R_{C_p}} \\
Q_{L_p} &= \frac{\omega_o L_p}{R_{L_p}}
\end{aligned}
\tag{4.7}
$$

These two parasitic resistances have the deterministic importance for the losses of the passive filter and the control of the active filter.

Since the active filter does not generate any fundamental voltage, the inverter capacitor is a short circuit for the fundamental current, and the funadmental voltage across the passive filter is the fundamental voltage at the PCC,

$$
v_{pf} = v_{Lf} = V_{Lf} \sin\left(\omega_o t + \phi_{v_{Lf}} \right) \tag{4.8}
$$

where V_{Lf} is the amplitude and $\phi_{v_{Lf}}$ is the phase angle of the PCC (load) voltage in reference to the phase A of source voltage which can be measured and assumed known.

With Equation (4.8), the current i_{pf} can be solved from Equations (4.3) and (4.5). For the current through the capacitor C_p

$$\begin{aligned} i_{C_p f} &= \frac{1}{\sqrt{R_{C_p}^2 + \left(\frac{1}{\omega_o C_p}\right)^2}} V_{Lf} \sin\left(\omega_o t + \phi_{v_{Lf}} + \frac{\pi}{2} - \tan^{-1}\omega_o C_p R_{C_p}\right) \\ &= I_{C_p f} \sin\left(\omega_o t + \phi_{i_{C_p f}}\right) \end{aligned} \tag{4.9}$$

and for the current through the inductor L_p

$$\begin{aligned} i_{L_p f} &= \frac{1}{\sqrt{R_{L_p}^2 + (\omega_o L_p)^2}} V_{Lf} \sin\left(\omega_o t + \phi_{v_{Lf}} - \tan^{-1}\frac{\omega_o L_p}{R_{L_p}}\right) \\ &= I_{L_p f} \sin\left(\omega_o t + \phi_{i_{L_p f}}\right) \end{aligned} \tag{4.10}$$

Since the parasitic resistances R_{C_p} and R_{L_p} are usually small, the arctangent terms in Equations (4.9) and (4.10) can be approximated as

$$\begin{aligned} \phi_{i_{L_p f}} &= \phi_{v_{Lf}} - \tan^{-1}\frac{\omega_o L_p}{R_{L_p}} \approx \phi_{v_{Lf}} - \frac{\pi}{2} \\ \phi_{i_{C_p f}} &= \phi_{v_{Lf}} + \frac{\pi}{2} - \tan^{-1}\omega_o C_p R_{C_p} \approx \phi_{v_{Lf}} + \frac{\pi}{2} \end{aligned} \tag{4.11}$$

As one would expect, the phase angle of the inductor current lags the voltage by $\pi/2$ and the phase angle of the capacitor current leads the voltage by $\pi/2$. Thus, $i_{L_p f}$ and $i_{C_p f}$ are almost out of phase to each other and the overall fundamental current through the passive filter, i_{pf}, is therefore insignificant. The exact i_{pf} can be calculated by summing the terms of Equations (4.9) and (4.10) as

$$
\begin{aligned}
i_{pf} &= i_{L_p f} + i_{C_p f} \\
&= \sqrt{I_{L_p f}^2 + I_{C_p f}^2 + 2I_{L_p f} \cdot I_{C_p f}\left(\cos\phi_{i_{L_p f}} \cdot \cos\phi_{i_{C_p f}} + \sin\phi_{i_{L_p f}} \cdot \sin\phi_{i_{L_p f}}\right)} \\
&\quad * \sin\left(\omega_o t + \tan^{-1}\frac{I_{L_p f}\sin\phi_{i_{L_p f}} + I_{C_p f}\sin\phi_{i_{C_p f}}}{I_{L_p f}\cos\phi_{i_{L_p f}} + I_{C_p f}\cos\phi_{i_{C_p f}}}\right) \\
&= I_{pf}\sin\left(\omega_o t + \phi_{i_{pf}}\right)
\end{aligned}
\tag{4.12}
$$

where I_{pf} is the magnitude and $\phi_{i_{pf}}$ is the phase angle of i_{pf}.

Although the current i_{pf} is very small, however, since the magnitude and phase angle of i_{pf} is actually determined by the mismatch between L_p and C_p and the parasitic resistances R_{L_p} and R_{C_p}, the approximation of Equation (4.11) is not valid for Equation (4.12) and the current i_{pf} must be calculated exactly by Equation (4.12).

With Equation (4.12), the first term on the right-hand side of Equation (4.1) is obtained. For the second terms concerning the current harmonics through the passive filter, $\Sigma_h i_{ph}$, the active filter is expected to work in a way that it will have all the load current harmonics $\Sigma_h i_{Lh}$ flow into the filter instead of the power line, that is,

$$
\sum_{h \neq 1} i_{ph} = -\sum_{h \neq 1} i_{Lh} \tag{4.13}
$$

The third term of Equation (4.1) is the main object of the active filtering. The voltage generated by the inverter is expected to equal the negative of the sum of harmonic voltages across the passive filter to make the PCC a harmonic ground.

Assume that the current harmonics are in the form of

$$
\sum_{h \neq 1} i_{ph} = \sum_{h \neq 1} I_{ph}\sin\left(h\omega_o t + \phi_{i_{ph}}\right) \tag{4.14}
$$

when the active filter is in action, all current harmonics produced by the load will be absorbed by the hybrid filter, that is,

$$\sum_{h\neq 1} i_{ph} = \sum_{h\neq 1} -I_{Lh}\sin\left(h\omega_o t + \phi_{i_{Lh}}\right) \tag{4.15}$$

The harmonic currents through C_p and L_p must sum up to i_{ph} as depicted by Equation (4.2),

$$i_{L_p h} = i_{ph} - i_{C_p h} \tag{4.16}$$

The capacitor current is chosen to express the inductor current since most harmonic currents will pass through the capacitor which has low impedances at high frequencies. Substituting Equations (4.5) and (4.16) into (4.4), the other relationship among the three current components is obtained:

$$\sum_{h\neq 1}\left(L_p C_p \frac{d^2}{dt^2} + C_p R_{L_p}\frac{d}{dt}\right) i_{L_p h} = \sum_{h\neq 1}\left(C_p R_{C_p}\frac{d}{dt} + 1\right) i_{C_p h} \tag{4.17a}$$

$$\sum_{h\neq 1}\left(L_p C_p \frac{d^2}{dt^2} + C_p R_{L_p}\frac{d}{dt}\right)\left(i_{ph} - i_{C_p h}\right) = \sum_{h\neq 1}\left(C_p R_{C_p}\frac{d}{dt} + 1\right) i_{C_p h} \tag{4.17b}$$

$$\begin{aligned}&\sum_{h\neq 1}\left(L_p C_p \frac{d^2}{dt^2} + C_p R_{L_p}\frac{d}{dt}\right) i_{ph}\\ &= \sum_{h\neq 1}\left(L_p C_p \frac{d^2}{dt^2} + C_p R_{L_p}\frac{d}{dt} + C_p R_{C_p}\frac{d}{dt} + 1\right) i_{C_p h}\end{aligned} \tag{4.17c}$$

With i_{ph} assumed known from Equation (4.14), the current $i_{C_p h}$ can be calculated from Equation (4.17c):

$$\sum_{h\neq 1}\left[-h^2\omega_o^2 L_p C_p \sin\left(h\omega_o t+\phi_{i_{ph}}\right)+h\omega_o C_p R_{L_p}\sin\left(h\omega_o t+\phi_{i_{ph}}+\frac{\pi}{2}\right)\right]I_{ph}$$
$$=\sum_{h\neq 1}\left[\left(1-h^2\omega_o^2 L_p C_p\right)\sin\left(h\omega_o t+\phi_{i_{C_p h}}\right)\right. \tag{4.18}$$
$$\left.+h\omega_o C_p\left(R_{L_p}+R_{C_p}\right)\sin\left(h\omega_o t+\phi_{i_{C_p h}}+\frac{\pi}{2}\right)\right]I_{C_p h}$$

The capacitor current can be explicitly expressed by combining the terms on each side of Equation (4.18) into only one term

$$\sum_{h\neq 1} h\omega_o C_p\sqrt{\left(h\omega_o L_p\right)^2+R_{L_p}^2}\,I_{ph}\sin\left(h\omega_o t+\phi_{i_{ph}}-\tan^{-1}\left(\frac{R_{L_p}}{h\omega_o L_p}\right)\right)$$
$$=\sum_{h\neq 1}\sqrt{\left(1-h^2\omega_o^2 L_p C_p\right)^2+h^2\omega_o^2 C_p^2\left(R_{C_p}+R_{L_p}\right)^2} \tag{4.19a}$$
$$*\,I_{C_p h}\cdot\sin\left(h\omega_o t+\phi_{i_{C_p h}}+\tan^{-1}\left(\frac{h\omega_o C_p\left(R_{C_p}+R_{L_p}\right)}{1-h^2\omega_o^2 L_p C_p}\right)\right)$$

hence,

$$\sum_{h\neq 1} i_{C_p h}=\sum_{h\neq 1}\frac{h\omega_o C_p\sqrt{\left(h\omega_o L_p\right)^2+R_{L_p}^2}}{\sqrt{\left(1-h^2\omega_o^2 L_p C_p\right)^2+h^2\omega_o^2 C_p^2\left(R_{C_p}+R_{L_p}\right)^2}}I_{ph}$$
$$*\sin\left(h\omega_o t+\phi_{i_{ph}}-\tan^{-1}\left(\frac{R_{L_p}}{h\omega_o L_p}\right)-\tan^{-1}\left(\frac{h\omega_o C_p\left(R_{C_p}+R_{L_p}\right)}{1-h^2\omega_o^2 L_p C_p}\right)\right) \tag{4.19b}$$
$$=\sum_{h\neq 1} I_{C_p h}\cdot\sin\left(h\omega_o t+\phi_{i_{C_p h}}\right)$$

where

$$I_{C_p h} = \frac{h\omega_o C_p \sqrt{(h\omega_o L_p)^2 + R_{L_p}^2}}{\sqrt{\left(1 - h^2\omega_o^2 L_p C_p\right)^2 + h^2\omega_o^2 C_p^2\left(R_{C_p} + R_{L_p}\right)^2}} I_{ph}$$
$$= \frac{h\omega_o C_p \sqrt{(h\omega_o L_p)^2 + R_{L_p}^2}}{\sqrt{\left(1 - h^2\right)^2 + h^2\omega_o^2 C_p^2\left(R_{C_p} + R_{L_p}\right)^2}} I_{ph} \tag{4.20a}$$

and

$$\phi_{i_{C_p h}} = \phi_{i_{ph}} - \tan^{-1}\left(\frac{R_{L_p}}{h\omega_o L_p}\right) - \tan^{-1}\left(\frac{h\omega_o C_p\left(R_{C_p} + R_{L_p}\right)}{1 - h^2}\right) \tag{4.20b}$$

for every h-th order of harmonics. Note that L_p and C_p are parallel-resonated at the fundamental frequency. Even considering the mismatch, still

$$\omega_o^2 L_p C_p \approx 1 \tag{4.21}$$

for high-quality power capacitors and inductors, the parasitic resistances are usually negligible, assuming

$$R_{C_p} \approx 0$$
$$R_{L_p} \approx 0 \tag{4.22}$$

the capacitor current can be simplified as

$$\sum_{h \neq 1} i_{C_p h} \approx \sum_{h \neq 1} \frac{1}{\left(1 - \frac{1}{h^2}\right)} I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}}\right)$$
$$= I_{C_p h} \sin\left(h\omega_o t + \phi_{i_{ph}}\right) \tag{4.23}$$

that is,

$$
\begin{aligned}
I_{C_p h} &\approx \frac{1}{\left(1-\frac{1}{h^2}\right)} I_{ph} \\
\phi_{i_{C_p h}} &\approx \phi_{i_{ph}}
\end{aligned}
\tag{4.24}
$$

From Equation (4.23), it is obvious that the higher order harmonic components of the filter current will pass mostly through the capacitor of the passive filter instead of the inductor, which is in accordance with basic circuit theory.

The third term concerning about the $\Sigma_h v_{ph}$ in Equation (4.1) can now be obtained by substituting Equation (4.19b) into (4.4):

$$
\begin{aligned}
&\sum_{h\neq 1} C_p \frac{d}{dt} v_{ph} = \sum_{h\neq 1} \left(1 + C_p R_{C_p} \frac{d}{dt}\right) i_{C_p f} \\
&\sum_{h\neq 1} h\omega_o C_p V_{ph} \sin\left(h\omega_o t + \phi_{v_{ph}} + \frac{\pi}{2}\right) \\
&= \sum_{h\neq 1} \left(\sin\left(h\omega_o t + \phi_{i_{C_p h}}\right) + h\omega_o C_p R_{C_p} \sin\left(h\omega_o t + \phi_{i_{C_p h}} + \frac{\pi}{2}\right)\right) I_{C_p h} \\
&= \sum_{h\neq 1} \sqrt{1 + \left(h\omega_o C_p R_{C_p}\right)^2} I_{C_p h} \sin\left(h\omega_o t + \phi_{i_{C_p h}} + \tan^{-1}\left(h\omega_o C_p R_{C_p}\right)\right)
\end{aligned}
\tag{4.25}
$$

thus,

$$
\begin{aligned}
\sum_{h\neq 1} v_{ph} &= \sqrt{R_{C_p}^2 + \left(\frac{1}{h\omega_o C_p}\right)^2} I_{C_p h} \\
&\quad * \sin\left(h\omega_o t + \phi_{i_{C_p h}} - \frac{\pi}{2} + \tan^{-1}\left(h\omega_o C_p R_{C_p}\right)\right) \\
&= \sum_{h\neq 1} V_{ph} \sin\left(h\omega_o t + \phi_{v_{ph}}\right)
\end{aligned}
\tag{4.26}
$$

where

$$
\begin{aligned}
V_{ph} &= \sqrt{R_{C_p}^2 + \left(\frac{1}{h\omega_o C_p}\right)^2} I_{C_p h} \\
\phi_{v_{ph}} &= \phi_{i_{C_p h}} - \frac{\pi}{2} + \tan^{-1}\left(h\omega_o C_p R_{C_p}\right)
\end{aligned}
\tag{4.27}
$$

for the h-th order of harmonics, or by Equation (4.24)

$$\sum_{h\neq 1} v_{ph} \approx \sum_{h\neq 1} \frac{1}{\left(h-\frac{1}{h}\right)(\omega_o C_p)} I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} - \frac{\pi}{2}\right) \tag{4.28}$$

From Equations (4.26) and (4.28), it is obvious that

$$\begin{aligned} |v_{ph}| &= V_{ph} \approx \frac{1}{\left(h-\frac{1}{h}\right)(\omega_o C_p)} I_{ph} \\ \phi_{v_{ph}} &\approx \phi_{i_{ph}} - \frac{\pi}{2} \end{aligned} \tag{4.29}$$

For a balanced 3ϕ system, the lowest possible order of harmonics is the 5th harmonic, so at least $h \geq 5$ and the magnitude of v_{ph} can be further simplified as

$$|v_{ph}| = V_{ph} \approx \frac{I_{ph}}{h\omega_o C_p} \tag{4.30}$$

Equation (4.30) implies that all the harmonic current passes through the capacitor C_p, which is a good approximation for the application.

With i_{pf} from Equation (4.12), $\Sigma_h i_{ph}$ from Equations (4.14) or (4.15), and $\Sigma_h v_{ph}$ from Equation (4.29), the duty ratio for the inverter can be explicitly written as

$$\begin{aligned} d_a i_{dc} &= -i_{pf} - \sum_{h\neq 1} i_{ph} - \sum_{h\neq 1} C_i \cdot \frac{dv_{ph}}{dt} \\ &= -I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}}\right) - \sum_{h\neq 1} I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}}\right) \\ &\quad - \sum_{h\neq 1} h\omega_o C_i V_{ph} \sin\left(h\omega_o t + \phi_{v_{ph}} + \frac{\pi}{2}\right) \end{aligned} \tag{4.31}$$

The two harmonic terms in Equation (4.31) can be combined into one unified term with a magnitude and a phase angle for each harmonic of order h as

$$
\begin{aligned}
d_a i_{dc} &= -I_{pf}\sin\left(\omega_o t + \phi_{i_{pf}}\right) - \sum_{h\neq 1}\sqrt{I_{ph}^2 + \left(h\omega_o C_i V_{ph}\right)^2 + 2C_{oeff}} \\
&\quad * \sin\left(h\omega_o t + \tan^{-1}\frac{I_{ph}\sin\left(\phi_{i_{ph}}\right) + h\omega_o C_i V_{ph}\sin\left(\phi_{v_{ph}} + \frac{\pi}{2}\right)}{I_{ph}\cos\left(\phi_{i_{ph}}\right) + h\omega_o C_i V_{ph}\cos\left(\phi_{v_{ph}} + \frac{\pi}{2}\right)}\right) \qquad (4.32) \\
&= -I_{pf}\sin\left(\omega_o t + \phi_{i_{pf}}\right) - \sum_{h\neq 1} I_{ph_{eff}}\sin\left(h\omega_o t + \phi_{i_{ph_{eff}}}\right)
\end{aligned}
$$

where

$$
\begin{aligned}
C_{oeff} = h\omega_o C_i V_{ph} I_{ph}\Big[&\cos\left(\phi_{i_{ph}}\right)\cos\left(\phi_{v_{ph}} + \frac{\pi}{2}\right) \\
&+\sin\left(\phi_{i_{ph}}\right)\sin\left(\phi_{v_{ph}} + \frac{\pi}{2}\right)\Big]
\end{aligned} \qquad (4.33a)
$$

and

$$
\begin{aligned}
I_{ph_{eff}} &= \sqrt{I_{ph}^2 + \left(h\omega_o C_i V_{ph}\right)^2 + 2C_{oeff}} \\
\phi_{i_{ph_{eff}}} &= \tan^{-1}\frac{I_{ph}\sin\left(\phi_{i_{ph}}\right) + h\omega_o C_i V_{ph}\sin\left(\phi_{v_{ph}} + \frac{\pi}{2}\right)}{I_{ph}\cos\left(\phi_{i_{ph}}\right) + h\omega_o C_i V_{ph}\cos\left(\phi_{v_{ph}} + \frac{\pi}{2}\right)}
\end{aligned} \qquad (4.33b)
$$

are the magnitude and phase angle of the equivalent harmonic component which the inverter needs to filter.

With Equations (4.29) and (4.30), Equation (4.32) can be further simplified as

$$
\begin{aligned}
C_{oeff} = h\omega_o C_i V_{ph} I_{ph} &\approx \frac{1}{1 - \frac{1}{h^2}}\frac{C_i}{C_p} I_{ph}^2 \\
&\approx \frac{C_i}{C_p} I_{ph}^2
\end{aligned} \qquad (4.34)
$$

$$I_{ph_{eff}} \approx \left(1 + \frac{1}{1 - \frac{1}{h^2}} \frac{C_i}{C_p} \right) I_{ph} \tag{4.35a}$$

and

$$\begin{aligned} \phi_{i_{ph_{eff}}} &\approx \tan^{-1} \frac{\sin \phi_{i_{ph}}}{\cos \phi_{i_{ph}}} \\ &= \tan^{-1} \left(\tan \phi_{i_{ph}} \right) \\ &= \phi_{i_{ph}} \end{aligned} \tag{4.35b}$$

From Equation (4.13) and (4.35), it is obvious that if all the assumptions are held valid, the duty ratio which is the direct control function of the inverter can be greatly simplified by rewriting Equation (4.32) as

$$\begin{aligned} d_a i_{dc} &\approx -I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} \right) - \sum_{h \neq 1} \left(1 + \frac{1}{1 - \frac{1}{h^2}} \frac{C_i}{C_p} \right) I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} \right) \\ &= -I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} \right) + \sum_{h \neq 1} \left(1 + \frac{1}{1 - \frac{1}{h^2}} \frac{C_i}{C_p} \right) I_{Lh} \sin\left(h\omega_o t + \phi_{i_{Lh}} \right) \\ &\approx -I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} \right) + \sum_{h \neq 1} \left(1 + \frac{C_i}{C_p} \right) I_{Lh} \sin\left(h\omega_o t + \phi_{i_{Lh}} \right) \end{aligned} \tag{4.36}$$

Since the input current i_{dc} is essentially a stable DC current with small switching ripples and the current I_{pf} is the mismatched fundamental current, which usually is very small even when the filter is not exactly tuned at the fundamental frequency as shown in Table 4-1, the control of the active filtering is directly proportional to the load current harmonics,

$$
\begin{aligned}
d_a &\propto \Sigma i_{Lh} \\
|d_a| &\propto \Sigma I_{Lh} \\
\phi_{d_{ah}} &= \phi_{i_{Lh}}
\end{aligned}
\tag{4.37}
$$

This simple relationship between the duty ratio and the load harmonic current that is expected to be eliminated leads to a very simple control scheme as shown in Figure 4.5. With the steady-state value of inverter input current i_{dc} known, all one needs to perform is to

(1) measure the load current and filter out the fundamental component,

(2) scale the remaining harmonics as a modulation signal,

(3) compare the modulation signal with a switching carrier, and

(4) use the output to control the switches.

Then, the inverter will function as an active filter, absorb all current harmonics, and eliminate voltage harmonics at the PCC.

Note this control advantage is valid only for the parallel LC passive filter resonated at the fundamental frequency and thus behaves as a capacitor at high frequencies. The conventional compound passive filters, which consist of 5th, 7th, and 11th (high pass) order of series-resonated LC filters that do not behave as capacitors at the corresponding high frequencies, do not enjoy the control advantage.

With Equation (4.36), the minimum input current can be found by the requirement of Equation (3.62). Assuming that $i_{dc} = I_{d_{min}}$, the restriction on d_a is

$$
|d_a| = \max \left| \frac{-I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}}\right) + \sum_{h \neq 1} \left(1 + \frac{C_i}{C_p}\right) I_{Lh} \sin\left(h\omega_o t + \phi_{i_{Lh}}\right)}{I_{d_{min}}} \right| \leq \frac{2}{3} \tag{4.38}
$$

hence

$$I_{d_{min}} \geq \frac{3}{2}\max\left|-I_{pf}\sin\left(\omega_o t + \phi_{i_{pf}}\right) + \sum_{h \neq 1}\left(1 + \frac{C_i}{C_p}\right)I_{Lh}\sin\left(h\omega_o t + \phi_{i_{Lh}}\right)\right| \tag{4.39}$$

$$\begin{aligned} d_a(t) &\approx \frac{1}{I_{d_{min}}}\left[-I_{pf}\sin\left(\omega_o t + \phi_{i_{pf}}\right) + \sum_{h \neq 1}\left(1 + \frac{C_i}{C_p}\right)I_{Lh}\sin\left(h\omega_o t + \phi_{i_{Lh}}\right)\right] \\ &= d_f\sin\left(\omega_o t + \phi_{i_{pf}}\right) + \sum_{h \neq 1} d_h\sin\left(h\omega_o t + \phi_{i_{Lh}}\right) \\ d_b(t) &\approx d_f\sin\left(\omega_o t + \phi_{i_{pf}} - \frac{2\pi}{3}\right) + \sum_{h \neq 1} d_h\sin\left(h\omega_o t + \phi_{i_{Lh}} - \frac{2\pi}{3}h\right) \\ d_c(t) &\approx d_f\sin\left(\omega_o t + \phi_{i_{pf}} + \frac{2\pi}{3}\right) + \sum_{h \neq 1} d_h\sin\left(h\omega_o t + \phi_{i_{Lh}} + \frac{2\pi}{3}h\right) \end{aligned} \tag{4.40}$$

for the close approximations of $d_a(t)$, $d_b(t)$, and $d_c(t)$.

For engineering practice, the approximation terms for the duty ratio d(t) in Equation (4.40) is the one used in control of the inverter to generate a voltage that cancels the voltage harmonics in Equation (4.29). With the effective duty ratios $d_a(t)$, $d_b(t)$, and $d_c(t)$ from the above equation, the actual duty ratios associated with the switches $S_{1a}/S_{1b}/S_{1c}$ and $S_{2a}/S_{2b}/S_{2c}$ can be obtained by Equation (3.59).

With $I_{d_{min}}$ known, the DC input voltage V_{dc} can be calculated by Equation (3.65). The voltage drop across the source inductor can be written as

$$L_d\frac{di_{dc}}{dt} = V_{dc} - [d_a v_a + d_b v_b + d_c v_c] - \left(R_{L_d} + 2R_{on}\right)i_{dc} - 2V_{don} \tag{4.41}$$

where v_a, v_b, and v_c are the phase voltage harmonics generated at the inverter output capacitors:

$$
\begin{aligned}
v_a &= \sum_{h\neq 1} v_{aih} = -\sum_{h\neq 1} v_{aph} = -\sum_{h\neq 1} V_{ph}\sin\left(h\omega_o t + \phi_{v_{ph}}\right) \\
&\approx -\sum_{h\neq 1} V_{ph}\sin\left(h\omega_o t + \phi_{i_{ph}} - \frac{\pi}{2}\right) = \sum_{h\neq 1} V_{ph}\sin\left(h\omega_o t + \phi_{i_{Lh}} - \frac{\pi}{2}\right) \\
v_b &= \sum_{h\neq 1} v_{bih} = -\sum_{h\neq 1} v_{bph} \approx \sum_{h\neq 1} V_{ph}\sin\left(h\omega_o t + \phi_{i_{Lh}} - \frac{\pi}{2} - \frac{2\pi}{3}h\right) \\
v_c &= \sum_{h\neq 1} v_{cih} = -\sum_{h\neq 1} v_{cph} \approx \sum_{h\neq 1} V_{ph}\sin\left(h\omega_o t + \phi_{i_{Lh}} - \frac{\pi}{2} + \frac{2\pi}{3}h\right)
\end{aligned}
\tag{4.42}
$$

since $\phi_{i_{ph}} = \phi_{i_{Lh}} + \pi$ according to Equation (4.13). The term R_{L_d} is the parasitic resistance of the source inductor L_d; R_{on} is the on-resistance of the semiconductor switch (such as power MOSFETs); and V_{don} is the on-drop of the diode. The coefficient 2 is required for R_{on} and V_{don} since there are always two switches and two diodes turned on at any instant, one from each of the two switching poles. If a semiconductor switch with on-drop voltage V_{swon} is used (such as power BJTs, MCTs and IGBTs), Equation (4.41) is rewritten as

$$
L_d\frac{di_{dc}}{dt} = V_{dc} - [d_a v_a + d_b v_b + d_c v_c] - R_{L_d} i_{dc} - 2(V_{swon} + V_{don}) \tag{4.43}
$$

From Equations (4.40) and (4.42), it is seen that

$$
d_a v_a + d_b v_b + d_c v_c = 0 \tag{4.44}
$$

The source current i_{dc} can be treated as the sum of two component: the DC constant current and the ripple caused by the PWM switching pattern. In the describing equations for the low-frequency inverter behavior, the switching ripple term is ignored and

$$
i_{dc} = I_{dc} = I_{d_{min}} \tag{4.45}
$$

Hence, the derivative terms in Equations (4.41) and (4.43) are zero and the equations can be rewritten as

$$V_{dc} = \left(R_{L_d} + 2R_{on} \right) \cdot I_{dc} + 2V_{don} \tag{4.46}$$

$$V_{dc} = R_{L_d} I_{dc} + 2 \left(V_{swon} + V_{don} \right) \tag{4.47}$$

respectively. The above equations indicate that the DC input voltage source is only required to overcome the losses in the inverter, which can be minimized by reducing the magnitude of I_{dc}. This is achieved by connecting the passive LC parallel-resonant filter in series with the inverter to avoid the fundamental current from circulating in the inverter circuitry.

The results of a PSpice® simulation of the current-fed active/ LC parallel passive filter employed in power system active filtering is shown are Figure 4.6. The duty ratio for the inverter is obtained by using the control method described in Figure 4.5. It is seen in Figures 4.6(a) and (b) that the hybrid filter does absorb most of the load current harmonics and keep the %THD of the source current and load point voltage low. The case of the power system without any filtering is shown in Figure 4.7 for comparison. From Figures 4.6(f) and (g), it is seen that most of current harmonics pass through the parallel capacitor as depicted by Equation (4.23), and the major function of the parallel inductor is to provide a fundamental current to offset the fundamental current in the capacitor hence permit no significant amount of fundamental current through the inverter in order to keep the losses in the inverter low. The inverter current rises according to the RL time constant of the inverter.

4.2. A Voltage-Fed Inverter as the Active Filter

To explain the operation of the voltage-fed active filter clearly, a voltage-fed active filter employed by the power system as shown in Figure 4.3 is redrawn in Figure 4.8. Note that only phase A of the inverter is shown, and all the subscripts "a"s denoting the phase A of the power system are omitted for notation simplicity.

The exact switching state-space equations for the voltage-fed inverter applied as an active filter can be derived in the same way as depicted in Section 3.2 and are not re-derived. Base on the balanced 3ϕ assumption, the low-frequency describing equations for the voltage-fed active/LC parallel passive filter can be written as

$$\begin{aligned} L\frac{di_a}{dt} &= d_a\frac{V_{dc}}{2} - \sum_{h\neq 1} v_{ih} \\ C\frac{d\sum_{h\neq 1} v_{ih}}{dt} &= i_a + \left(i_{pf} + \sum_{h\neq 1} i_{ph}\right) \end{aligned} \tag{4.49}$$

Substituting $v_{ph} = -v_{ih}$ into Equation (4.49)

$$\begin{aligned} L\frac{di_a}{dt} &= d_a\frac{V_{dc}}{2} + \sum_{h\neq 1} v_{ph} \\ C_i\frac{d\sum_{h\neq 1} v_{ph}}{dt} &= -i_a - \left(i_{pf} + \sum_{h\neq 1} i_{ph}\right) \end{aligned} \tag{4.50}$$

and combining the two items of the above equation solves the required duty ratio for the inverter

$$\begin{aligned} LC_i\frac{d^2\sum_{h\neq 1} v_{ph}}{dt^2} &= -L\frac{di_a}{dt} - L\frac{di_{pf}}{dt} - L\frac{d\sum_{h\neq 1} i_{ph}}{dt} \\ &= -d_a\frac{V_{dc}}{2} - \sum_{h\neq 1} v_{ph} - L\frac{di_{pf}}{dt} - L\frac{d\sum_{h\neq 1} i_{ph}}{dt} \end{aligned} \tag{4.51}$$

With Σi_{pf}, Σi_{ph}, and Σv_{ph} in the forms found in Equations (4.13), (4.14), and (4.26), respectively, the duty ratio d_a for the voltage-fed inverter can be calculated as

$$\begin{aligned} d_a \frac{V_{dc}}{2} = & -(\omega_o L)\, I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} + \frac{\pi}{2}\right) \\ & - \sum_{h \neq 1} (h\omega_o L)\, I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} + \frac{\pi}{2}\right) \\ & - \sum_{h \neq 1} \left(1 - h^2 \omega_o^2 L C_i\right) V_{ph} \sin\left(h\omega_o t + \phi_{v_{ph}}\right) \end{aligned} \tag{4.52}$$

With the harmonic voltage and phase angle (V_{ph} and $\phi_{v_{ph}}$) across the LC parallel passive filter defined in Equation (4.29), the two harmonic terms can be greatly simplified and combined into one as

$$\begin{aligned} d_a \frac{V_{dc}}{2} \approx & -(\omega_o L)\, I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} + \frac{\pi}{2}\right) \\ & - \sum_{h \neq 1} (h\omega_o L)\, I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} + \frac{\pi}{2}\right) \\ & - \sum_{h \neq 1} \frac{\left(1 - h^2 \omega_o^2 L C_i\right)}{\left(h - \frac{1}{h}\right)\omega_o C_p} I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} - \frac{\pi}{2}\right) \end{aligned} \tag{4.53}$$

$$\begin{aligned} d_a \frac{V_{dc}}{2} \approx & -(\omega_o L)\, I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} + \frac{\pi}{2}\right) \\ & - \sum_{h \neq 1} \left[h\omega_o L - \frac{\left(1 - h^2 \omega_o^2 L C_i\right)}{\left(h - \frac{1}{h}\right)\omega_o C_p} \right] I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} + \frac{\pi}{2}\right) \end{aligned}$$

Comparing Equation (4.53) with (4.36),

(1) The individual harmonic component of the duty ratio for a current-fed inverter is proportional to the respective harmonic current, which leads to a very simple control scheme and can be implemented with a simple analog operational amplifier circuit as shown in Figure 4.5.

(2) The magnitude of the individual harmonic duty ratio for a voltage-fed active filter is related to inductance and capacitance of the inverter, as well as the magnitude of the specific harmonic. The phase angle of the individual harmonic duty ratio is leading to the corresponding harmonic current by almost $\pi/2$. Hence, the duty ratios can be obtained only by the feedback control procedure shown in Figure 4.9 or a microprocessor-based control scheme with the voltage-mode control. The current-mode control [65] of a voltage-fed inverter can be done by generating the duty ratios from the errors between the output inductor current i_a (i_b and i_c) and the line harmonic current. In this case, some local feedback is still required for the active filtering to function correctly.

Since $|d_a| \le 1$ for a voltage-fed inverter, the minimum DC voltage for the active filter to work is

$$V_{dc_{min}} = 2*\min\left| \begin{array}{l} (\omega_o L)\, I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} + \frac{\pi}{2}\right) \\ + \sum_{h \neq 1} \left[h\omega_o L - \frac{\left(1 - h^2 \omega_o{}^2 L C_i\right)}{\left(h - \frac{1}{h}\right)\omega_o C_p} \right] I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} + \frac{\pi}{2}\right) \end{array} \right| \qquad (4.54)$$

and the effective duty ratio is

$$d_a(t) \approx \frac{2}{V_{dc_{min}}} \left[\begin{array}{l} (\omega_o L)\, I_{pf} \sin\left(\omega_o t + \phi_{i_{pf}} - \frac{\pi}{2}\right) \\ + \sum_{h \neq 1} \left[h\omega_o L - \frac{\left(1 - h^2 \omega_o{}^2 L C_i\right)}{\left(h - \frac{1}{h}\right)\omega_o C_p} \right] I_{ph} \sin\left(h\omega_o t + \phi_{i_{ph}} - \frac{\pi}{2}\right) \end{array} \right] \qquad (4.55)$$

The other two effective duty ratios $d_b(t)$ and $d_c(t)$ are in the same form as $d_a(t)$ but with a

phase shift of 120^0 to one another. The actual duty ratios associated with the switches S_{a1}/S_{a2}, S_{b1}/S_{b2}, and S_{c1}/S_{c2} of the voltage-fed inverter can be obtained from Equation (3.49).

The feasibility of the voltage-fed inverter for the active/passive filter employed in the power system filtering is shown by PSpice® simulation in Figure 4.10. Note that the simulation is "open-looped" with effective duty ratios calculated from Equation (4.55). The real dynamic responses of the hybrid filter will be certainly different when a closed-loop control scheme is employed.

With the load current harmonics known, the MATLAB® script files for calculating the DC current/voltage and open-loop duty ratios for the current-fed and voltage-fed inverters are listed in Appendices B.1 and B.2, respectively. For any power system and load condition, the load current harmonics with PCC voltage truly sinusoidal can be obtained by the PSpice® file listed in Appendix A.12.

4.3. Loss Mechanisms and Power Ratings of the Active/Passive Hybrid Filters

4.3.1. Loss Mechanisms

Since the current-fed inverter does not inject any real power into the power system, the power provided by the DC power source is all dissipated as losses in the inverter circuitry. The product of inverter current and voltage, P_{inv}, is the loss of the inverter

$$P_{inv} = V_{dc} \cdot I_{dc} \tag{4.56}$$

The DC current is calculated by Equation (4.39) and the voltage is obtained by Equation (4.46) or (4.47). Note from Equation (4.39) that I_{dc} is a function of the passive

filter capacitance C_p, and hence is the function of the inductance L_p. By ignoring the mismatched fundamental current in Equation (4.39), I_{dc} can be rewritten as

$$\begin{aligned} I_{dc} &\approx \frac{3}{2}\left(1+\frac{C_i}{C_p}\right)\cdot \max \sum_{h\neq 1}\left|I_{Lh}\sin\left(h\omega_o t+\phi_{i_{Lh}}\right)\right| \\ &= \frac{3}{2}\left(1+\omega^2{}_o L_p C_i\right)\cdot \max \sum_{h\neq 1}\left|I_{Lh}\sin\left(h\omega_o t+\phi_{i_{Lh}}\right)\right| \\ &= K\left(1+\omega^2{}_o L_p C_i\right) \propto L_p \end{aligned} \tag{4.57}$$

where $K = \frac{3}{2}\max \sum_{h\neq 1}\left|I_{Lh}\sin\left(h\omega_o t+\phi_{i_{Lh}}\right)\right|$ is a constant for a fixed load.

The losses in the three parallel-resonant filters supplied by the power system can be calculated from

$$\begin{aligned} P_{pas} &= \frac{3}{2}V_{Lf}I_{pf}\cos\left(\phi_{v_{Lf}}-\phi_{i_{pf}}\right) \\ &= \frac{3}{2}\left(I^2_{L_p f}\cdot R_{L_p}+I^2_{C_p f}\cdot R_{C_p}\right) \\ &\approx \frac{3}{2}I^2_{L_p f}\left(R_{L_p}+R_{C_p}\right) \\ &= \frac{3}{2}\left(\frac{V_{Lf}}{\omega_o L_p}\right)^2\left(R_{L_p}+R_{C_p}\right) \end{aligned} \tag{4.58}$$

The total loss of the hybrid filter is

$$P_{tot} = P_{inv} + P_{pas} \tag{4.59}$$

From Equations (4.10), (4.57), and (4.58), it is seen that the $\omega_o L_p$ factor of P_{inv} is in the numerator and this factor is in the denominator for P_{pas}; thus, a minimum overall loss in the hybrid filter is possible by setting

$$\frac{\partial P_{tot}}{\partial \omega_o L_p} = 0 \tag{4.60}$$

and solve the $\omega_o L_p$ (or $\omega_o C_p$) analytically. The other method to find the $\omega_o L_p$ (or $\omega_o C_p$) for a minimum loss is to plot Equation (4.59) versus $\omega_o L_p$ (or $\omega_o C_p$) and find the minimum graphically.

In order to assess the conduction losses in the hybrid filter, the realistic component parameters of the passive filter and the inverter must be used for the loss calculation because the voltage and current ratings of each individual component dramatically affect the losses. A 3kW 3ϕ full-bridge diode rectifier, which will be the prototype system for the experiment presented in the next chapter, is shown in Figure 4.11 with all parameters listed. With all the harmonic currents known, the conduction losses of the hybrid filter can be computed.

For a current-fed inverter, the filter capacitance C_p determines not only the DC current of the inverter but also the voltage across the inverter switch when it is OFF as shown in Figure 4.2 and Equations (4.26) and (4.36). The minimum blocking voltage rating V_{block} of the inverter switches must be at least equal to the possible maximum voltage across the inverter switch as

$$\begin{aligned} \min\left|V_{block}\right| &\geq \max\left|v_a - v_b\right| \\ &= \sqrt{3}\max\left|v_a\right| \\ &= \sqrt{3}\max\left|\sum_{h\neq 1} v_{ph}\right| \propto L_p\,(C_p) \end{aligned} \tag{4.61}$$

and the minimum current rating of the switch is I_{dc} in Equation (4.45).

For a voltage-fed inverter, the DC voltage of the inverter shown in Equation (4.54) is the minimum blocking voltage rating V_{block} for its switches. The current rating of the switch can be obtained solving the inductor current term in Equation (4.50). Both the

voltage and current ratings are related to the selection of C_p as shown in the equations.

By choosing the value of C_p and the components of the inverter properly, the overall losses can be minimized either in the case of current-fed inverter or the case of voltage-fed inverter. Figure 4.12 shows the ratings of V_{block} and I_{dc} and the losses versus the values of C_p for the current-fed inverter-based hybrid filter. Figure 4.13 shows the ratings of V_{block} and I_{dc} and the losses versus the values of C_p for a voltage-fed inverter-based hybrid filter. The curves in both figures are normalized with the bases of 3kW, 120V, and 8.33A for the power, voltage, and current, respectively, as shown in Figure 4.11. They are computed by the MATLAB® scripts listed in Appendix B. The quality factors of 100 and 50 are assumed for the passive capacitor C_p and the passive inductor L_p, respectively. Note that if the six-stepped PWM [43] is employed in the current-fed inverter, the inverter losses can be reduced by $(2/3)^2$ which is 44.4%

From Figure 4.12(a), it is seen clearly that larger C_p is desirable to reduce the current I_{dc} and the voltage V_{block}. However, a larger C_p means a smaller L_p, and the loss in the passive filter increases as shown in Figure 4.12(b). Thus, a trade-off must be made to have the lowest overall losses in the filter and the inverter.

If C_p= 150μF is chosen, the filter loss P_{ac} is 1.88% p.u. (56.4W), the inverter current I_{dc} is 2.10% p.u. (17.5A), and the minimum blocking voltage V_{block} of the switch is 28.75% p.u. (34.5V). A suitable MOSFET for these ratings is the HiperFET™ IXFH76N07-12 n-channel MOSFET from the IXYS, Co. with 70V blocking voltage (BV_{DSS}), 76A maximum drain current (I_D), and 12mΩ maximum on-resistance ($R_{DS(on)}$). The inverter diode holds the same V_{block} and I_{dc} requirements as the switch. Low on-drop

(V_{on}) Schottky diode should be used to reduce the conduction losses. From the International Rectifier, Co., the Schottky diode 40CPQ060 with 60V V_{RRM} with 40A I_F and 0.49V V_{on} can meet the voltage and current requirements of the inverter. With the chosen MOSFET and diode, the inverter conduction loss P_{inv} is 0.82% p.u. (24.5W) and the total loss P_{tot} is 2.7% p.u. (80.9W). The loss in the DC inductor is ignored. From Figure 4.13(a), it is seen that the chosen semiconductor devices for the current-fed inverter are also suitable for the voltage-fed inverter, and the inverter conduction loss P_{inv} is only 0.08% p.u. (2.4W) and the total loss P_{tot} is 1.96% p.u. (57W).

The overall losses of the two types of hybrid filters are listed in Table 4-2. The losses of the conventional compound series-resonant passive filters in series with a current-fed inverter is also listed for comparison. The capacitances C_5, C_7, and C_{11} for the series-tuned filter are the same and set equal to 1/3 C_p to have approximately the same total fundamental current in both passive filters. Note that for the current-fed inverter, the choices of semiconductor switches are critical for the inverter losses. For example, if the IGBT IRGPC50F (700V/60A/1.6V_{swon}) and diode MUR3040PT (600V/15Ax2/1.3V_{don}) are employed as the switches, the inverter loss P_{inv} will be 3.34% p.u. (100.4W) instead of 0.82% p.u. in Table 4-2.

From Table 4-2, it is seen that the voltage-fed inverter has the lowest overall losses when it is in series with the parallel-resonant filter. However, for a 3kW load, the current-fed inverter loses less than 1% of the output power and has the advantage of control simplicity. It is also obvious from Table 4-2 that, when the current-fed inverter is in series with the parallel-resonant filter, its loss does not increase with the increase of the passive

filter capacitances as in the case of the compound series-resonant filters being in series with it. Thus, when a current-fed inverter is employed for the role of active filter, the only choice of passive filters is the parallel-resonant filter in order to avoid high losses and have design flexibility.

Besides the control simplicity, the magnetic material requirements for the inductor of the parallel-resonant filter are less strict than the inductors of the series-resonant filter. Since there are full harmonic (wide-band) currents flowing through the series-resonant inductors, the harmonic voltages across the inductors will not be exactly opposite to the voltages across the corresponding capacitors if they are distorted due to the poor quality magnetic cores of the inductors. Thus, the inverter is required to generate higher harmonic voltages to have the hybrid filters function correctly and the losses in the inverter will increase. The parallel-resonant inductor is not required to have the wide-band capacity since most of the current harmonics bypass through the capacitor, and the harmonic voltages are dependent on the capacitor.

4.3.2. Power Ratings

With the prototype system shown in Figure 4.11, the VA ratings of the filter inductor and capacitor can be explicitly calculated. The VA ratings of the capacitor and inductor of the parallel-tuned filter in each phase can be computed as

$$\begin{aligned} S_{C_p} &= V_{L_{f_rms}} \cdot I_{C_{p_rms}} \\ &\approx \frac{1}{2} \cdot \sqrt{V^2_{L_f} + \sum_{h \neq 1} V^2_{ph}} \cdot \sqrt{I_{C_{pf}} + \sum_{h \neq 1} I^2_{C_{ph}}} \\ S_{L_p} &= V_{L_{f_rms}} \cdot I_{L_{p_rms}} \\ &\approx \frac{1}{2} \sqrt{V^2_{L_f} + \sum_{h \neq 1} V^2_{ph}} \cdot I_{C_{pf}} \end{aligned} \tag{4.62}$$

where V_{L_f}, $I_{C_{pf}}$, and $I_{C_{ph}}$ are the peak values, and the effect of the parasitic resistances are ignored. The fundamental current in the inductor is approximately equal to the capacitor fundamental current. With the current harmonics information in Figure 4.11, the normalized VA ratings of the capacitor and inductor versus the capacitance are plotted in Figure 4.14(a). The VA ratings for the compound series-resonant filter can be computed as

$$\begin{aligned} S_{C_s} &= S_{C_5} + S_{C_7} + S_{C_{11}} \\ &\approx \frac{1}{2} \cdot \left(\sqrt{V_{L_f}^2 + V_{C_5}^2} \cdot \sqrt{I_{C_f}^2 + I_{C_5}^2} + \sqrt{V_{L_f}^2 + V_{C_7}^2} \cdot \sqrt{I_{C_f}^2 + I_{C_7}^2} \right. \\ &\quad \left. + \sqrt{V_{L_f}^2 + \sum_{h>7} V_{C_h}^2} \cdot \sqrt{I_{C_f}^2 + \sum_{h>7} I_{C_h}^2} \right) \qquad (4.63) \\ S_{L_s} &= S_{L5} + S_{L7} + S_{L11} \\ &\approx \frac{1}{2} \cdot \left(I_{C_f}^2 + 5I_{C_5}^2 \right) \omega_o L_5 + \left(I_{C_f}^2 + 7I_{C_5}^2 \right) \omega_o L_7 + \left(I_{C_f}^2 + 7I_{C_5}^2 \right) \omega_o L_{11} \end{aligned}$$

It is assumed that all filters have the same capacitance value to have the same amount of fundamental current. The 11th series-resonant filter also serves as the high pass filter with a resistor in parallel with L_{11} as shown in Figure 2.5. The VA ratings of the capacitors and inductors are plotted in Figure 4.14(b) for the compound series resonant filters.

From Figure 4.14, it is seen that the capacitors' VA ratings are about the same if the total capacitances in each filter are the same. However, series-resonant filters have low inductor VA ratings while the inductor VA rating of the parallel-resonant filter is equal to the rating of its associated capacitor. Thus, the total ratings of the parallel-resonant filter are about two times the ratings of the compound series-resonant filters.

The VA rating of the inverter is equivalent to its loss since it does not inject power into the system. As discussed in Section 4.3.1 and shown in Table 4-2, the inverter VA rating for the parallel-resonant filter is always less than the inverter rating of the

compound series-resonant filters. Also, in contrast with the case of the series-resonant filters, the parallel-resonant filter has the advantage of changing the component values flexibly without increase the losses in the inverter, since the inverter VA rating of the parallel-resonant filter is not significantly affected by the capacitance changes of the passive filter.

4.4. Total Harmonic Distortion Errors Due to the Open-Loop Control

Based on Equation (4.36), the open-loop control scheme in Figure 4.5 assumes that all current harmonics pass through the parallel-resonant capacitor and R_{C_p} is zero. The discrepancies between the real and the assumed situations need further investigation to validate the assumption. Table 4-3 is a list of the magnitudes and phase angles of the parallel-resonant filter with different C_p. It is seen from the table and Equation (4.26) that the ESR R_{C_p} of C_p is the deterministic factor for the phase differences. The lower the R_{C_p} is, the closer the real situation and the assumption is. By choosing C_p= 150μF to active filter the system in Figure 4.11, the harmonic distortions of the load voltage V_L, caused by the impedance discrepancies, are 0.67%, 0.26%, and 0.20% for the 5th, 7th, and 11th harmonic, respectively. The %THD for V_L due to the impedance errors is 0.75%, which is very small. Thus, the assumption for the open-loop control in Equation (4.36) and Figure 4.5 is valid. Besides the difference between the assumed and the real filter impedances, the sources for the residue %THD of V_L are (1) the phase delays caused by the current sensors, (2) the amplitude and phase distortions caused by the OP AMP circuitry, and (3) the PWM operations of the inverter [43].

Based on the analysis in Sections 4.1 and 4.3, an active filtering experiment with a 3kW 3ϕ full-bridge diode rectifier shown in Figure 4.11 has been done. The experimental setup and results are presented in the next chapter.

Table 4-1. The fundamental current I_f through the parallel-resonant LC passive filter.

nominal parameters / I_f (p.u.) / L_p variations	C_p= 50μF L_p= 140.7mH	C_p= 150μF L_p= 46.9mH
110% L_p	2.59%	7.76%
100% L_p	0.81%	2.44%
90% L_p	3.14%	9.41%
	27.15% without L_p	81.46% without L_p

1. V_{base}= 120V_{rms} and I_{base}= 8.33A_{rms}.
2. The quality factors Q_{C_p} = 100 and Q_{L_p} = 50 .
3. Variations in L_p equivalent to 95% - 105% of the fundamental frequency changes

Table 4-2. A loss and control comparison among different filter configurations.

	5th-7th-11th Series + current-fed $C_{5,7,11}$=50μF	5th-7th-11th Series + current-fed $C_{5,7,11}$=100μF	5th-7th-11th Series + current-fed $C_{5,7,11}$=150μF	Fundamental Parallel + current-fed C_p=150μF	Fundamental Parallel + current-fed C_p=300μF	Fundamental Parallel + current-fed C_p=450μF	Fundamental Parallel + voltage-fed C_p=150μF
Passive filter loss (%p.u.)	1.08%	2.67%	5.09%	1.88%	3.78%	5.66%	1.88%
Active filter conduction loss (%p.u.)	2.09%	3.01%	5.34%	0.82%	0.68%	0.62%	0.08%
Overall losses (%p.u.)	3.17%	5.68%	10.43%	2.70%	4.46%	6.28%	1.96%
Control Simplicity	Complex	Complex	Complex	Simple	Simple	Simple	Complex

1. P_{base}= 3kW, V_{base}= 120V, and I_{base}= 8.33A as shown in Figure 4.11.
2. C_i=100μF.
3. L_i= 0.2mH for the voltage-fed inverter.
4. IXYS HiperFET™ IXFH76N07-12 n-channel MOSFET BV_{DSS}= 70V, I_D= 76A, and $R_{DS(on)}$= 12mΩ used.
5. Schottky diode 40CPQ060: V_{RRM}= 60V, I_F =40A, and V_{on}=0.49V used.

Tbale 4-3. The impedances of the parallel-resonant filter.

	$Z_5 \angle Z_5\ \Omega$		$Z_7 \angle Z_7\ \Omega$		$Z_{11} \angle Z_{11}\ \Omega$	
	actual	assumed	actual	assumed	actual	assumed
50μF	11.07∠–87°	10.61∠–90°	7.76∠–85.9°	7.58∠–90°	4.89∠–83.7°	4.82∠–90°
100μF	5.53∠–87°	5.31∠–90°	3.88∠–85.9°	3.79∠–90°	2.45∠–83.7°	2.41∠–90°
150μF	3.69∠–87°	3.54∠–90°	2.58∠–85.9°	2.53∠–90°	1.63∠–83.7°	1.61∠–90°
200μF	2.77∠–87°	2.65∠–90°	1.94∠–85.9°	1.89∠–90°	1.22∠–83.7°	1.21∠–90°
$Q_{C_p} = 100$ and $Q_{L_p} = 50$						

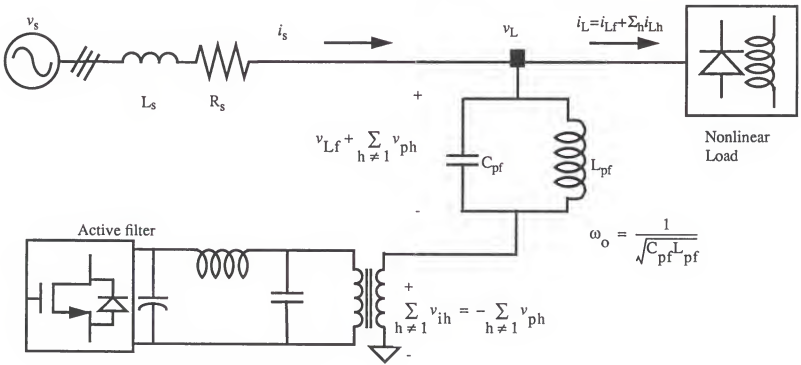


Figure 4.1. The proposed active/passive hybrid filter for harmonic eliminations employing low-ratings inverter.

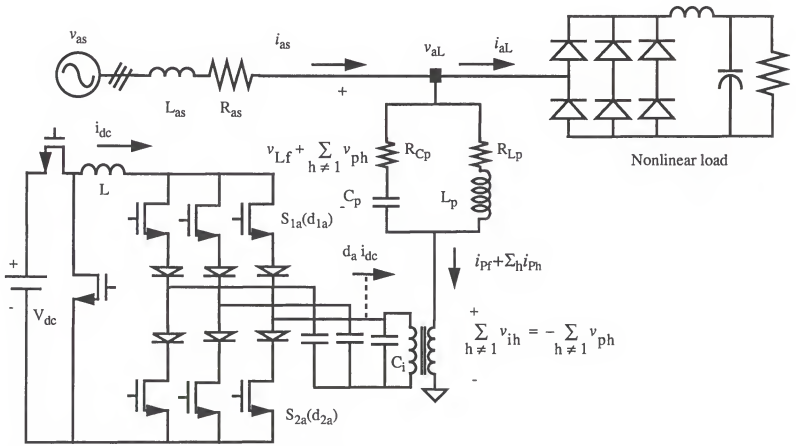


Figure 4.2. The current-fed inverter as the active filter in the proposed active/passive hybrid filter for nonlinear load harmonic elimination.

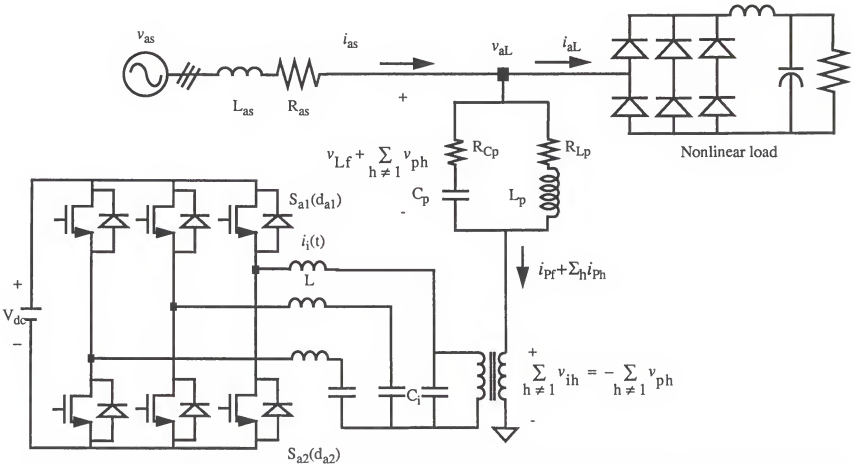


Figure 4.3. The voltage-fed inverter as the active filter in the proposed active/passive filter for nonlinear load harmonic elimination.

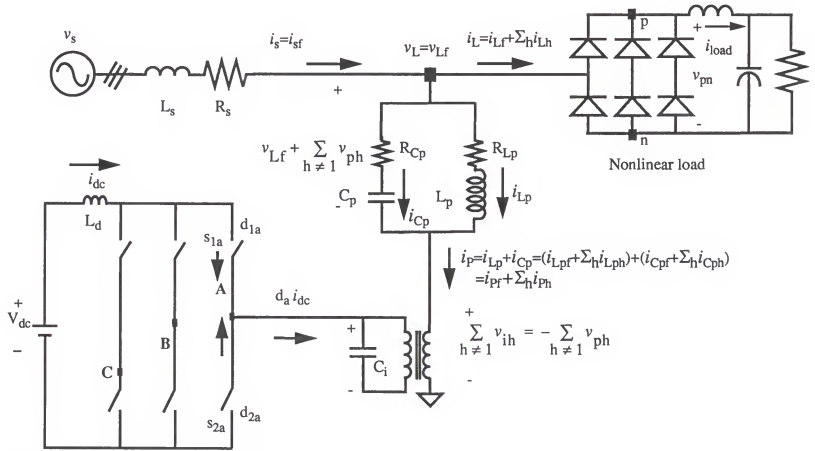


Figure 4.4. The schematic sketch of a current-fed inverter as the active filter in the proposed hybrid filter for harmonic elimination. Only one phase is shown and all subscripts indicating phases for the power system are omitted to simplify the notations.

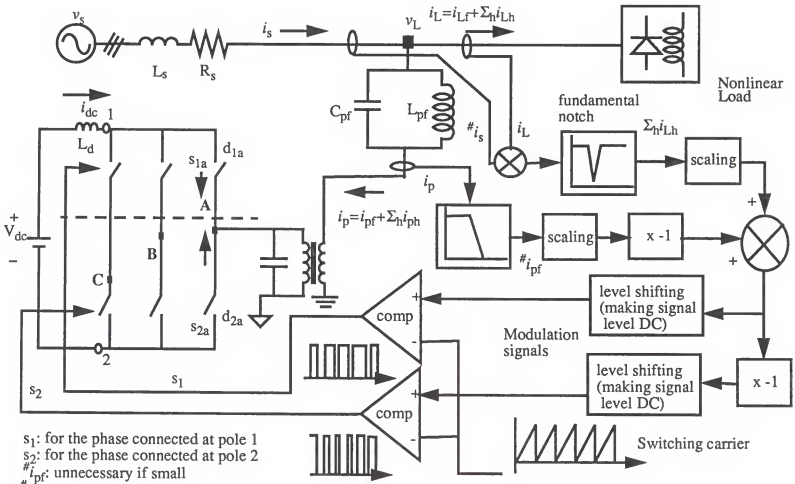


Figure 4.5. The schematic control diagram for the active filtering employing current-fed inverter as shown in Figures 4.2 and 4.4.

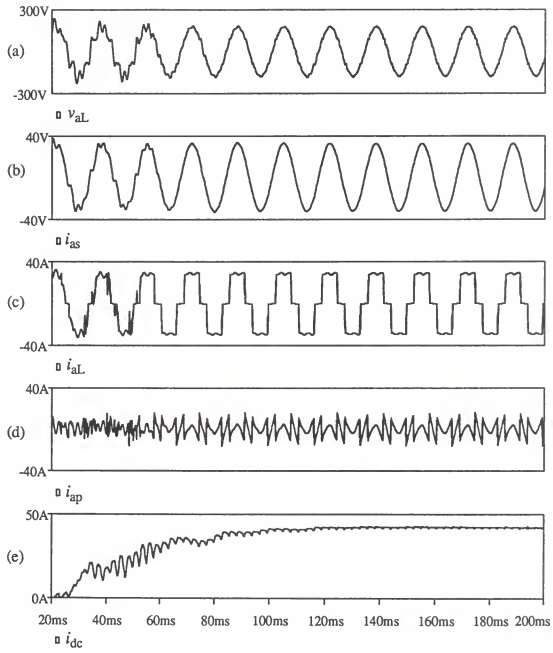


Figure 4.6. Active filtering employed the hybrid current-fed active/LC parallel-resonant passive filter described in Figure 4.5 (all for phase A).

(a) The load voltage at PCC v_L;

(b) The power line current i_s;

(c) The load current i_L;

(d) The current through the parallel passive filter $i_{ap} \propto d_a$;

(e) The DC current of the inverter i_{dc};

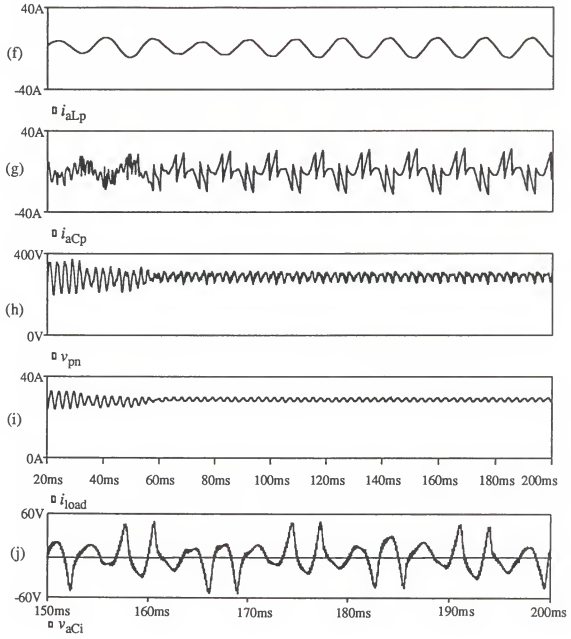


Figure 4.6 (continued).

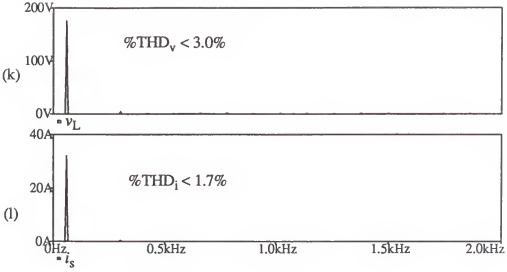
(f) The current through the passive filter inductor i_{Lp};

(g) The current through the passive filter capacitor i_{Cp};

(h) The voltage across the rectifier v_{pn};

(i) The current through the rectifier load inductor i_{load};

(j) The A-phase harmonic voltage generated by the active inverter v_{Ci};



Variables	Parameters
Source voltage v_s	208V
Line Inductance L_s	4.573mH
Line resistance R_s	0.7372Ω
Load inductance L_x	10mH
Load capacitance C_x	50μF
Load resistance R_{load}	10Ω
Parallel filter inductance L_f	46.91mH
Parallel filter capacitance C_f	150μF
Quality factor of L_f	20
Switching Frequency	8kHz
Inverter voltage v_{dc}	8.4V
Inverter inductance L_{dc}	10mH
Inverter capacitance C_i	100μF
PSpice® circuit file in Appendix A.9.	

Figure 4.6 (continued).
(k) The spectrum of v_L in (a);
(l) The spectrum of i_s in (b).

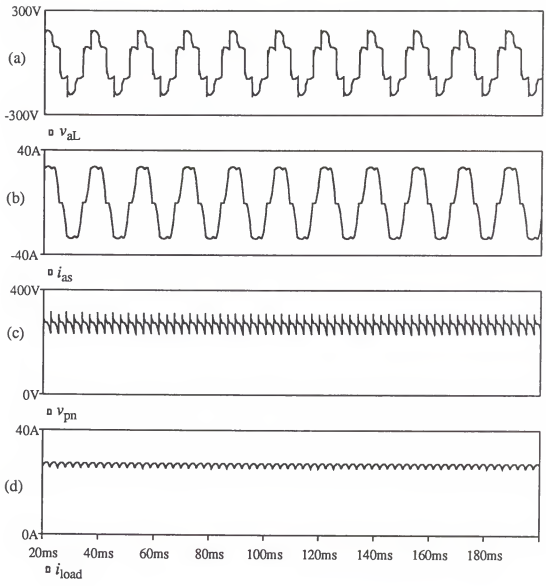


Figure 4.7. The power system with the same 3ϕ rectifier load as in Figure 4.6, but without any filtering (all for phase A).
(a) The load voltage at PCC v_L;
(b) The power line current i_s;
(c) The voltage across the rectifier v_{pn};
(d) The current through the rectifier load inductor i_{load}.

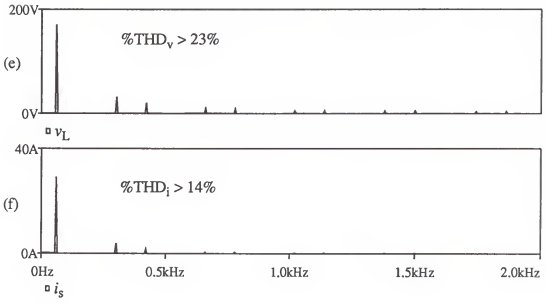


Figure 4.7 (continued).
(e) The spectrum of v_L in (a);
(f) The spectrum of i_s in (b).

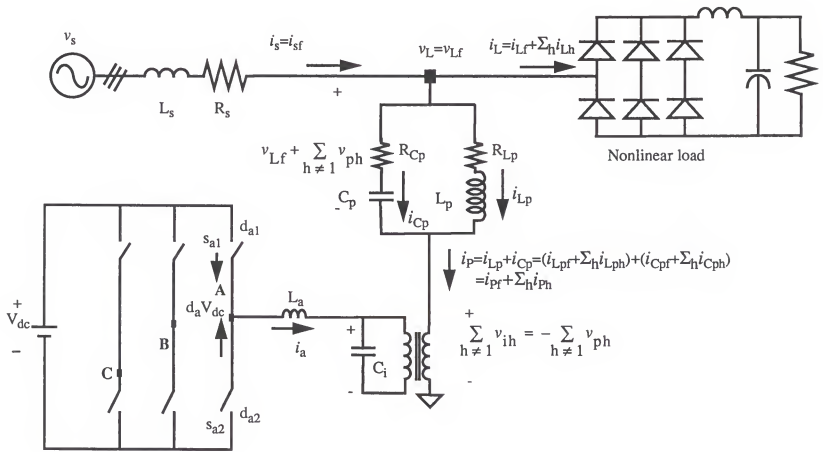
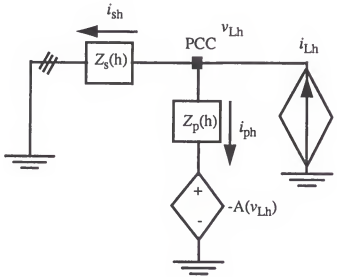


Figure 4.8.The schematic sketch of a voltage-fed inverter as the active filter in the proposed hybrid filter for harmonic elimination. Only one phase is shown and all subscripts indicating phases for the power system are omitted to simplify the notations.



$$i_{sh} = \frac{v_{Lh}}{Z_s(h)}$$

$$i_{ph} = \frac{(1+A)\,v_{Lh}}{Z_p(h)}$$

$$i_{Lh} = i_{sh} + i_{ph}$$

$$= \frac{v_{Lh}}{Z_s(h)} + \frac{(1+A)\,v_{Lh}}{Z_p(h)}$$

$$= \frac{(1+A)\,Z_s(h) + Z_p(h)}{Z_s(h)\,Z_p(h)}\,v_{Lh}$$

$$\therefore v_{Lh} = \frac{Z_s(h)\,Z_p(h)}{(1+A)\,Z_s(h) + Z_p(h)}\,i_{Lh}$$

A: negative feedback gain.

Figure 4.9. The harmonic diagram and active filtering employing a voltage-fed inverter.

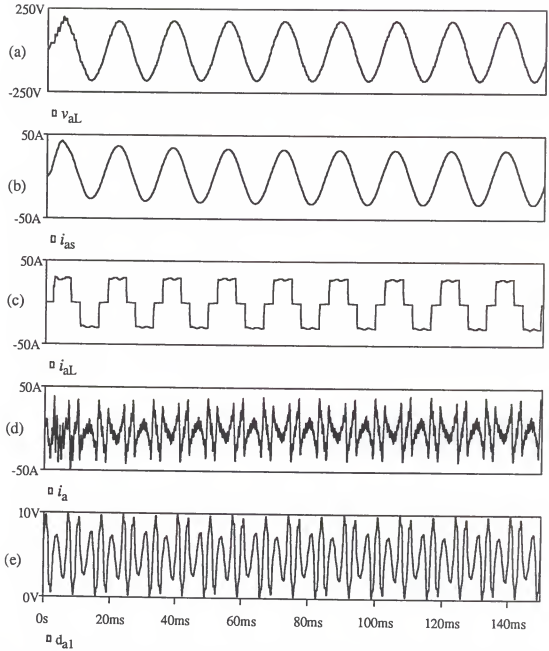


Figure 4.10. Active filtering employed the hybrid voltage-fed active/LC parallel-resonant passive filter with open-loop duty ratios d_a, d_b, and d_c calculated from Appendix B.2 (all for phase A).

(a) The load voltage at PCC v_L;

(b) The power line current i_s;

(c) The load current i_L;

(d) The current through the inverter inductor i_a;

(e) The duty ratio d_{a1} for switch throw S_{a1}.

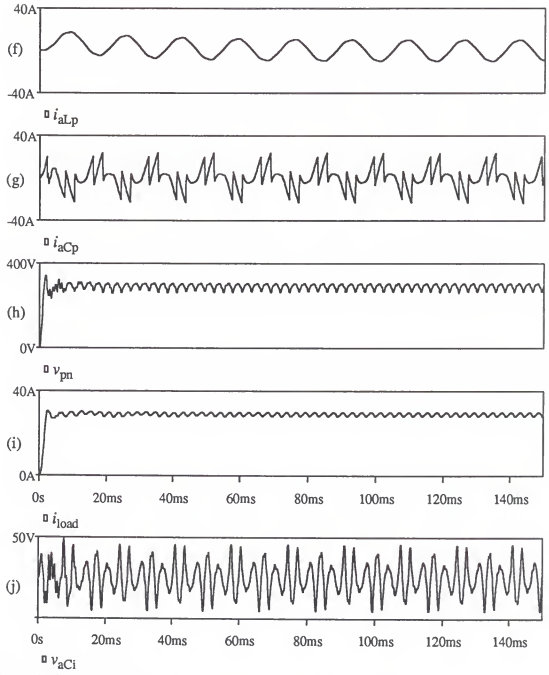


Figure 4.10 (continued).

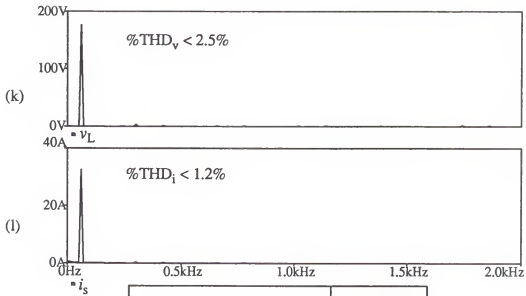
(f) The current through the passive filter inductor i_{Lp};

(g) The current through the passive filter capacitor i_{Cp};

(h) The voltage across the rectifier v_{pn};

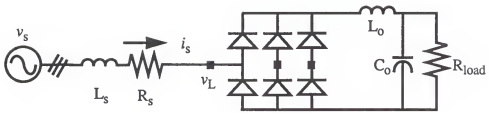
(i) The current through the rectifier load inductor i_{load};

(j) The A-phase harmonic voltage generated by the active inverter v_{Ci};



Variables	Parameters
Source voltage v_s	208V
Line Inductance L_s	4.573mH
Line resistance R_s	0.7372Ω
Load inductance L_x	10mH
Load capacitance C_x	50μF
Load resistance R_{load}	10Ω
Parallel filter inductance L_f	46.91mH
Parallel filter capacitance C_f	150μF
Quality factor of L_f	20
Switching Frequency	8kHz
Inverter voltage v_{dc}	62V
Inverter inductance L_{dc}	0.1mH
Inverter capacitance C_i	200μF
PSpice® circuit file in Appendix A.11.	

Figure 4.10 (continued).
(k) The spectrum of v_L in (a);
(l) The spectrum of i_s in (b).



Power system setup

Parameter	Value
Source voltage v_s	3ϕ $120V_{LNrms}$
Line inductance L_s	4.572mH
Line resistance R_s	0.7372Ω
Rectifier load R_{load}	21.9Ω
Rectifier filter inductance L_o	5mH
Rectifier filter capacitance C_o	50μF
Power base	3kW
Voltage base	120V
Current base	8.33A

For v_L containing fundamental only

Harmonic Current	Peak Value (A)
5th	3.353 (-17.72°)
7th	1.673 (-76.17°)
11th	1.319 (115.0°)
13th	0.942 (56.62°)

Figure 4.11. The system for computing the conduction losses in the hybrid filter.

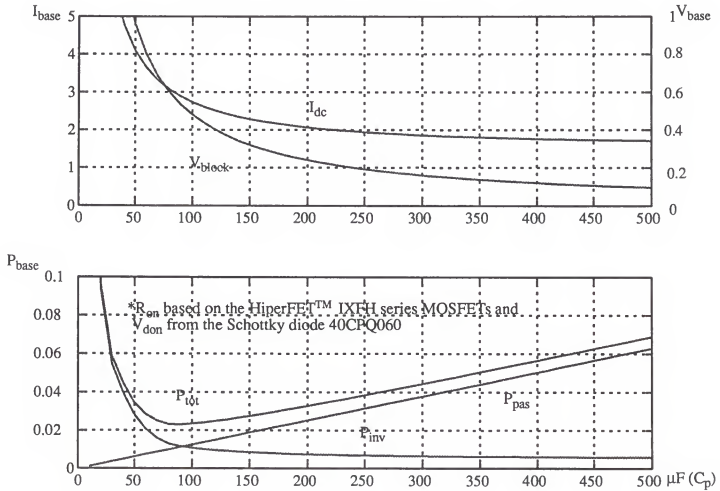


Figure 4.12. The voltage-ampere ratings of the current-fed inverter switches (a) and the losses of the hybrid filter (b).

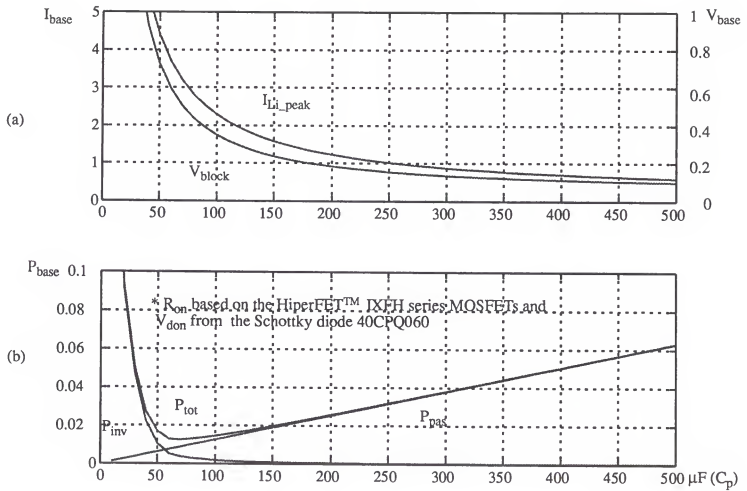


Figure 4.13. The voltage-ampere ratings of the voltage-fed inverter switches (a) and the losses of the hybrid filter (b).

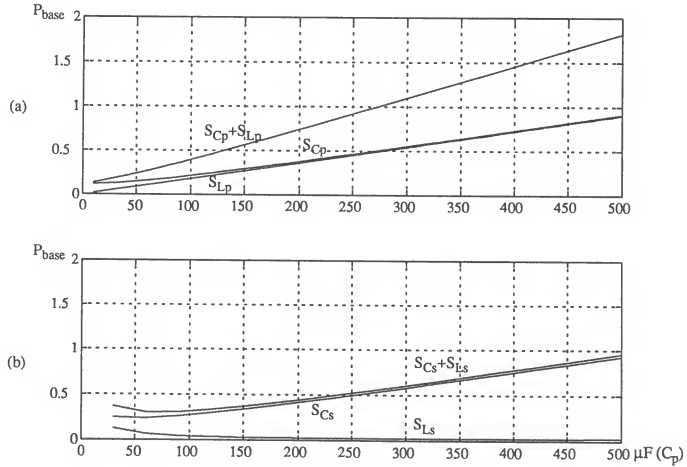


Figure 4.13. The voltage-ampere ratings of the parallel-resonant filter (a) and the series-resonant filter (b).

CHAPTER 5
EXPERIMENTAL RESULTS OF A TEST SYSTEM

A prototype of 3ϕ distribution system with 3kW diode rectifier load has been built to test the feasibility of the hybrid current-fed active/parallel-resonant passive filters. The experimental setup is shown in Figure 5.1; the electrical parameters are listed in Table 5-1; and the components are listed in Table 5-2.

The differences between Figures 4.1 and 5.1 are

(1) there is no DC side buck converter in Figure 5.1,

(2) the isolation transformer is omitted in Figure 5.1 for simplicity,

(3) the switching devices are IGBTs instead of MOSFETs in the experiment, and

(4) the IGBT is paralleled with a diode to provide a path for the reverse recovery current of the diode in series with the IGBT.

The control circuit of the current-fed inverter, schematically drawn in Figure 4.5, consists of current sensors and operational amplifier circuitry shown in Figures 5.2 to 5.6. Figure 5.2 shows a biquad circuit that eliminates the 60Hz component [66, 67] sensed by the current sensors. The biquad circuit shown in Figure 5.3 is coupled with a second-order Butterworth filter to filter out the 10KHz switching frequency component without introducing significant phase shift on the desired low harmonic frequencies. The transfer function of the circuit in Figure 5.2 is

$$\frac{a_1(s)}{i_{La}(s)} = -5\left(1 + \frac{1/R^2{}_1C^2{}_1}{s^2 + (1/R_1C_1)s + 1/R^2{}_1C^2{}_1} \cdot \frac{s - 1/R_2C_2}{s + 1/R_2C_2}\right)$$
$$= -5\left(1 + \frac{\omega^2{}_{c1}}{s^2 + (\omega_{c1})s + \omega^2{}_{c1}} \cdot \frac{s - \omega_{c2}}{s + \omega_{c2}}\right) \qquad (5.1)$$

where ω_{c1} = 384.6 rad/s and ω_{c2} = 362.3 rad/s. Equation (5.1) acts as a 60Hz notch filter because the second term provides an out-of-phase 60Hz component to cancel the component in the sensed load current. The transfer function of the circuit in Figure 5.2 is

$$\frac{a_2(s)}{a_1(s)} = -3.63\left(1 - \frac{2}{3}\frac{s/R_3C_3 + 1/R_3R_5C^2{}_3}{s^2 + (1/R_4C_3)s + 1/R^2{}_5C^2{}_3}\right)$$
$$*\frac{1/R^2{}_6C_4C_5}{s^2 + (2/R_6C_4)s + 1/R^2{}_6C_4C_5} \qquad (5.2)$$
$$= -3.63\left(1 - \frac{2}{3}\frac{(R_4/R_3)(\omega_{c1}/Q_3)s + H\omega^2{}_{c3}}{s^2 + (\omega_{c1}/Q_3)s + \omega^2{}_{c3}}\right)\frac{\omega^2{}_{c4}}{s^2 + (\omega_{c4}/Q_4)s + \omega^2{}_{c4}}$$

where ω_{c3} = 15151 rad/s, Q_3 = 0.55, H=0.7, ω_{c4} = 14857 rad/s, and Q_4 = 2. The function of the first term in Equation (5.2) is to provide some compensation for the phase lost to the low-pass filtering of the second term. The Bode plot of $a_2(s)/i_{La}(s)$ is shown in Figure 5.7.

After being processed by Equations (5.1) and (5.2), the sensed currents now become the duty ratio references $d_a(t)$ and $d_b(t)$ and are ready for level shifting and pulse-width-modulating to drive the inverter as shown in Figures 5.4 to 5.6. Note that the time axis indicates only a period time lapse instead of the actual operating time starting at zero second.

The experimental results are shown in Figures 5.8 to 5.20. Figures 5.8 and 5.9 show the load point (PCC) voltage, v_L, and the distribution line current, i_s, of the 3kW loaded diode rectifier without any filtering. The total harmonic distortions of the v_L and i_s are shown in Figure 5.10.

Figures 5.11 and 5.12 show the 3ϕ load voltage, v_L, and line current, i_s, when the proposed active/passive hybrid filter is in action. It can be seen that the voltage harmonics are greatly reduced and the voltage profile is almost sinusoidal. This proves the feasibility of the current-fed inverter to be employed as an active filter. The total harmonic distortions of v_L and i_s in this case are shown in Figure 5.13. The load voltage, line current, and load current for one phase are shown in Figure 5.14. The passive filter currents are shown in Figure 5.15. From Figures 5.14 and 5.15, it is seen clearly that most of the load current harmonics flow through the passive filter, but the net fundamental current through the filter is small.

Figures 5.16 and 5.17 show the switching waveforms of the inverter. These waveforms demonstrate typical PWM behavior. The voltage spike that occurs at the instant of the switch being turned off is caused by the inductance of the DC source. If the voltage spike is so high that it will destroy the switch, a small RC snubber in parallel with the switch can reduce the spikes. Since the blocking voltage across the switch is small and determined by Equation (4.61), a low blocking voltage semiconductor switch with a suitable current rating can be used. The low current rating devices can even be paralleled if the current requirement is high. Since it is the intrinsic property of the semiconductor devices that if the VA rating is low, conduction losses also will be low, the inverter efficiency can be improved. The harmonic voltages generated at the output capacitors of

the inverter, shown in Figure 5.18, also depict that the voltage ratings of the semiconductor devices can be low when the passive filter blocks all the fundamental voltages.

The comparison between the passive filter current, i_p, and the duty ratio function, $d_{1a}(t)$, is shown in Figure 5.19. Ideally, $d_{1a}(t)$ should be the exact replica of i_p with proper DC level. Because $d_{1a}(t)$ is obtained by sensing the load current with a current sensor and then processed through the notch and low-pass circuitry made of operational amplifiers, due to the propagation delays and the phase compensation action in the circuitry, the discrepancy is inevitable and the load current harmonics can not be 100% completely absorbed by the filter. However, the active filtering performance is very good with this type of open-loop control.

Figure 5.20 shows the power rectifier output voltage with and without active filtering for comparison. It is seen that the removal of line current and load voltage harmonics can increase the power output ability of a power system since the output voltage across the full-bridge rectifier is higher in the case of active filtering; hence, the power losses in the inverter and the passive filter are not wasted in vain.

Table 5-3 lists the output power and losses in the inverter and the passive filter. The overall loss is about 4.61% of the output power in this experiment. The loss in the current-fed inverter is high because the IGBTs and diodes used in this experiment are high voltage devices, and have high on-drop voltages. However, if the low rating devices described in Section 4.3 are employed, the loss will be greatly reduced.

The experiment has proven the current-fed hybrid filter's ability to perform active filtering on power systems with a much simpler control requirement.

Table 5-1: Experimental parameters of the mimic power system with active filtering.

Parameter	Value
Source voltage v_s	3ϕ $120V_{LNrms}$
Line inductance L_s	7mH @ 60Hz MagneTek C-59U/2
Line resistance R_s	60mΩ
Rectifier load R_{load}	21.9Ω
Rectifier filter inductance L_o	5mH MagneTek C-59Ux3
Rectifier filter capacitance C_o	50μF
Passive filter inductance L_p	42mH MagneTek C-59Ux1
R_{L_p} of L_p	120mΩ
Passive filter capacitance C_p	100μF
ESR R_{C_p} of C_p	50mΩ
Inverter inductance L_d	4.67mH
Inverter current I_{dc}	20A
Inverter voltage V_{dc}	5.8V
Control circuit supply voltage	+15 & -15V

Table 5-2: The components of the experiment.

Component	Type
Inductor	MagneTek C-59U (10mH @ 12.5Adc) MagneTek C-60U (5mH @ 22.5Adc)
capacitor	MALLORY (50uF/370Vac)
IGBT	IRGPC50F (700V/60A)
Parallel diode	MUR160 (600V/1A)
Inverter diode	MUR3040 (600V/15Ax2)
3ϕ diode rectifier	CRYDOM B485C-2 (240Vac/50A)
Inverter power source	Sorenson DCR150-15A x2
Current sensor	F.W.BELL BB-100 (100A/60KHz, 20:1)
OP AMP	LM833N
Comparator	LM393N
Buffer	DS0026
Opto isolator	HCPL3100
Switching Reference signal	Philips PM5192 function generator (10KHz ramp)

Table 5-3: The power and losses of the experiment

	Output	Inverter	Passive filter
Watt	3086	116	25.5
p.u.	100%	3.76%	0.85%

$$P_{out} = V_{out}^2 / R_{load} = 260^2 / 21.9$$

$$P_{inv} = V_{dc} \cdot I_{dc} = 5.8 \times 20$$

$$P_{pas} = \frac{3}{2} I_{L_p f}^2 \left(R_{L_p} + R_{C_p} \right)$$

$$= \frac{3}{2} 10^2 (0.12 + 0.05)$$

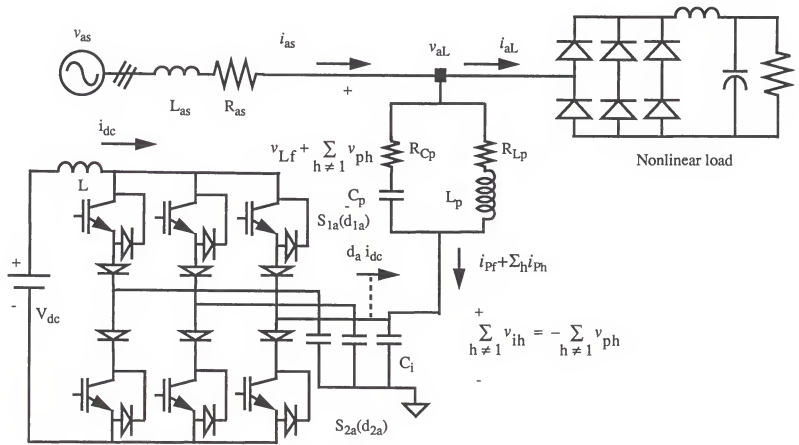


Figure 5.1. The experimental setup.

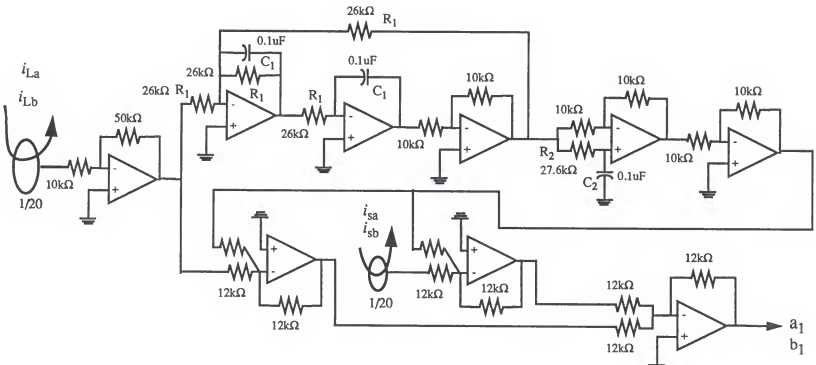


Figure 5.2. The control circuit for removing the fundamental signals from the current spectrum.

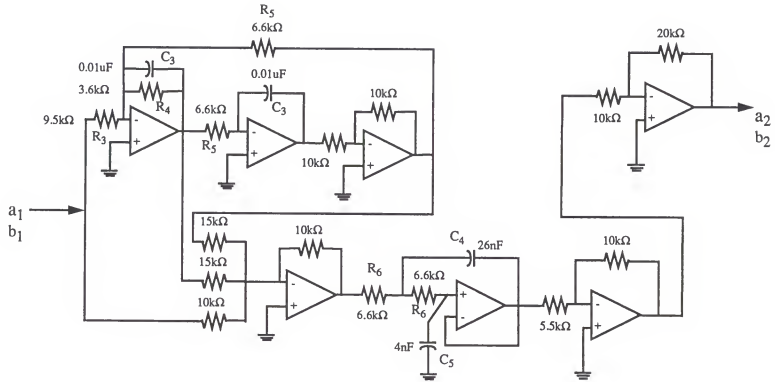


Figure 5.3 The control circuit for removing the switching noise without introducing large phase-distortion at desired harmonic frequencies.

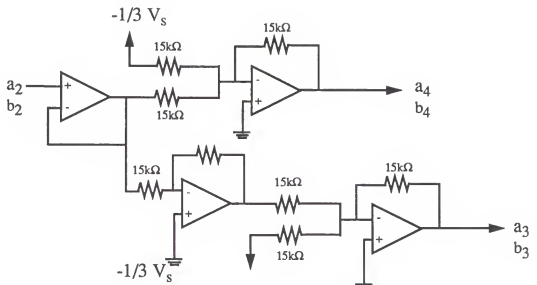


Figure 5.4. The control circuit for level shifting the duty ratio signals for switches S_{1a} and S_{2a}.

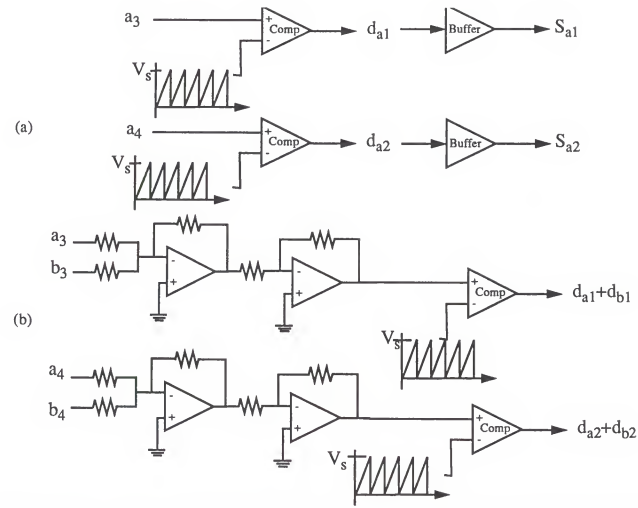


Figure 5.5. The control circuit generating the switching drives for S_{1a} and S_{2a} (a) and for level shifting the duty ratio signals for switches S_{1b} and S_{2b} (b).

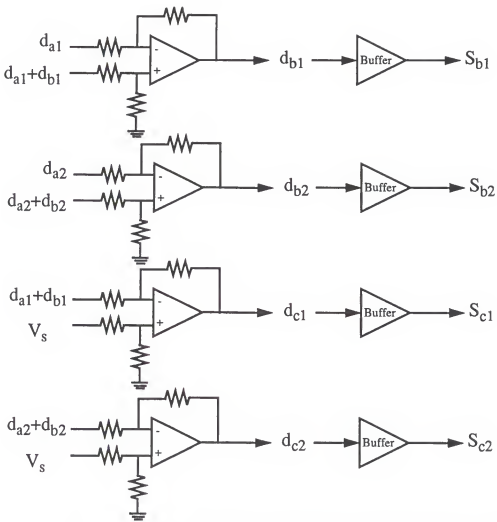


Figure 5.6. The control circuit generating the switching drives for S_{1b} /S_{2b} and S_{1c} /S_{2c}.

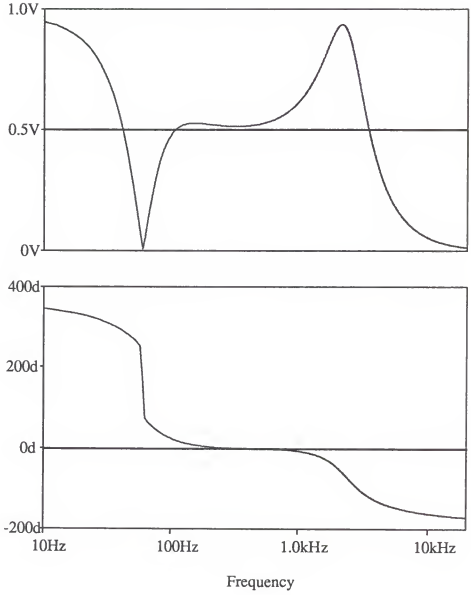


Figure 5.7. The PSpice simulation of the transfer function of the duty ratio control circuit.

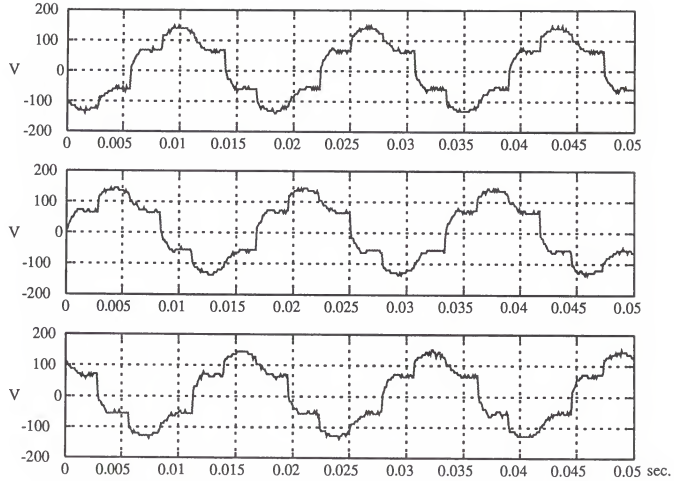


Figure 5.8. The load (PCC) voltages of the prototype system without any filtering.

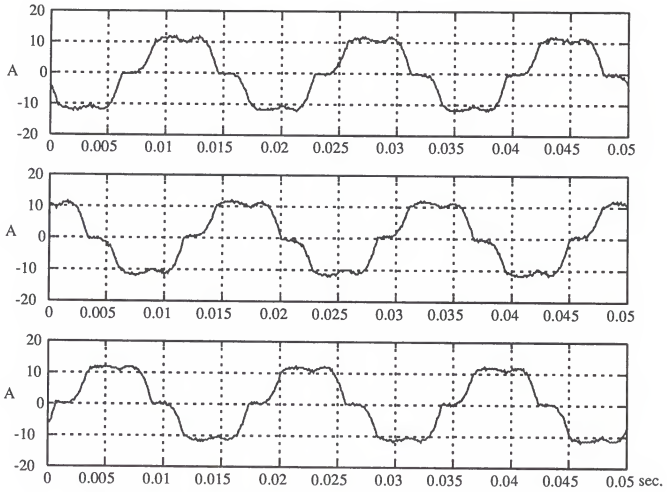


Figure 5.9. The distribution line currents without any filtering.

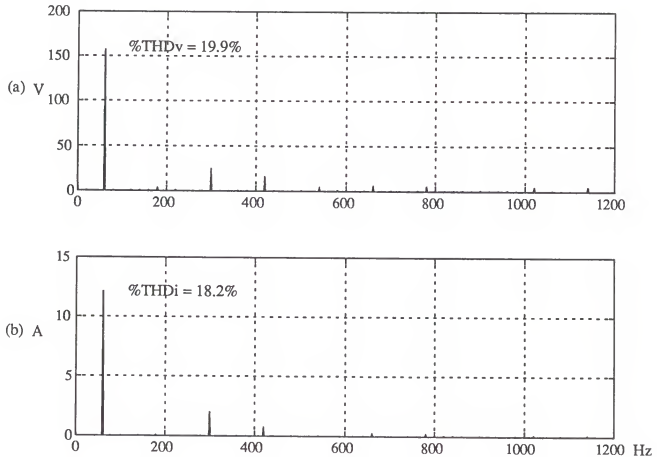


Figure 5.10. The %THDof the load voltage (a) and line current (b) of Figures 5.8 and 5.9, respectively.

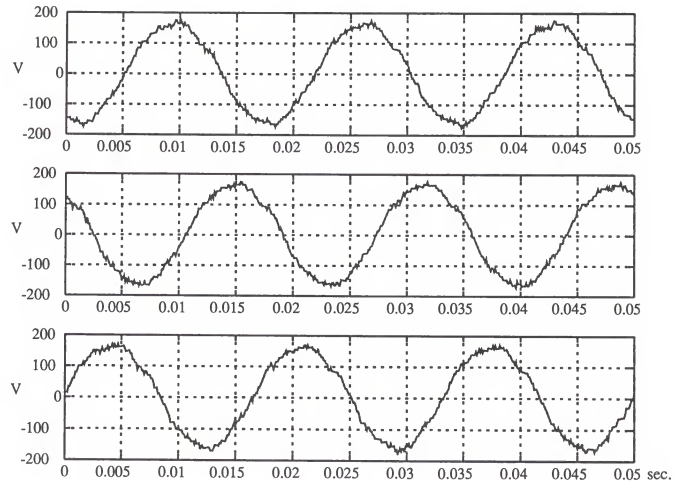


Figure 5.11. The load (PCC) voltage with the hybrid active/passive filter in action.

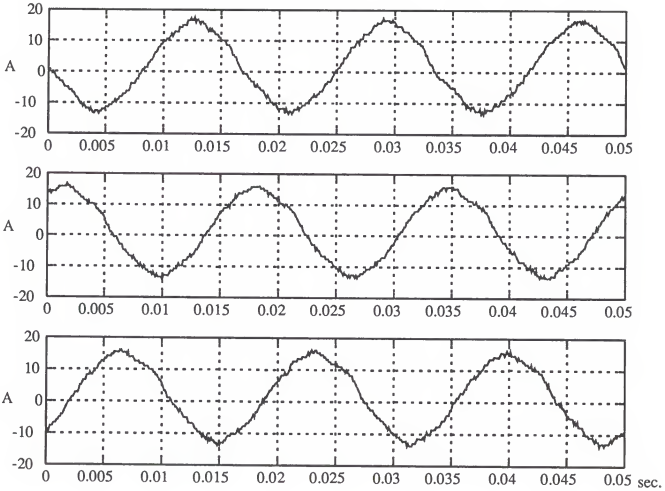


Figure 5.12. The line current with the hybrid active/passive filter in action.

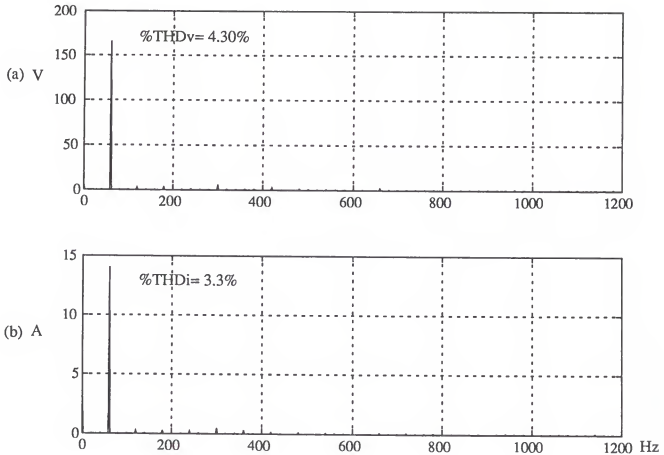


Figure 5.13. The total harmonic distortion of the load voltage (a) and line current (b) of Figures 5.11 and 5.12, respectively.

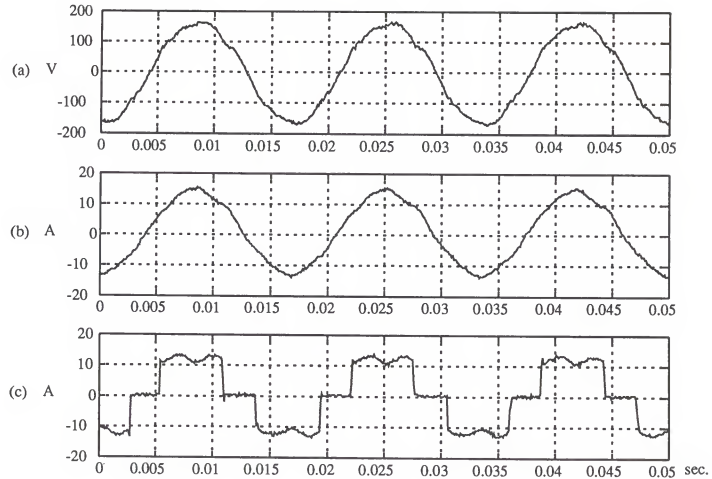


Figure 5.14. The load (PCC) voltage (a), line current (b), and load current (c) with the hybrid filter being in action.

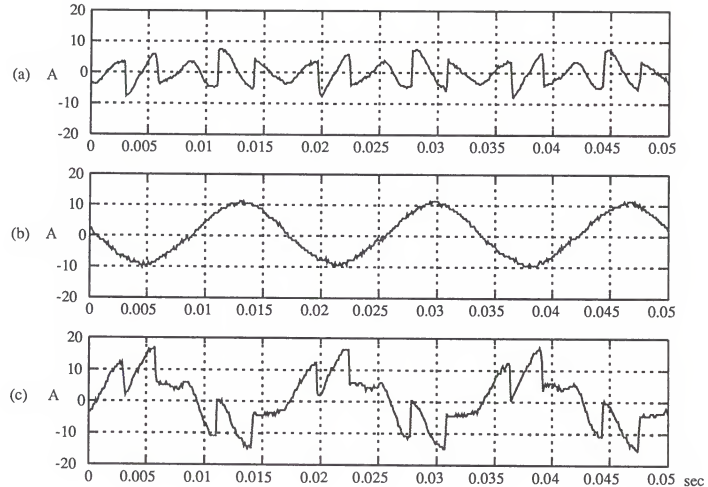


Figure 5.15. The passive filter current i_p (a), the current through the inductor i_{Lp} (b), and the current through the capacitor i_{Cp} (c).

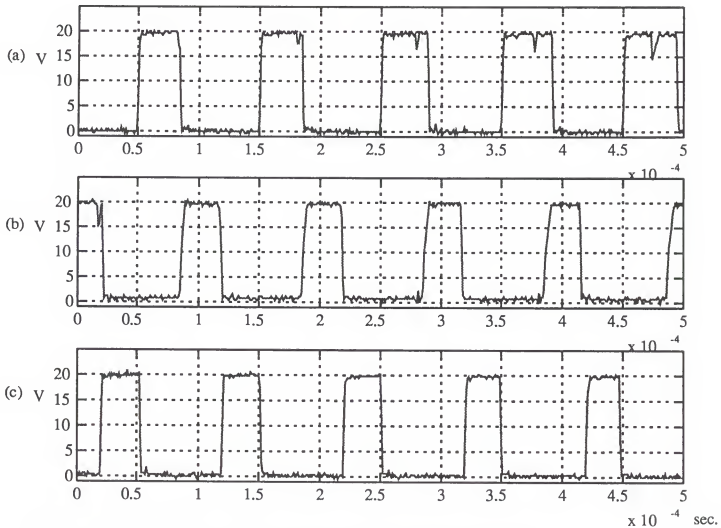


Figure 5.16. The inverter current through switches S_{1a} (a), S_1b (b), and S_{1c} (c).

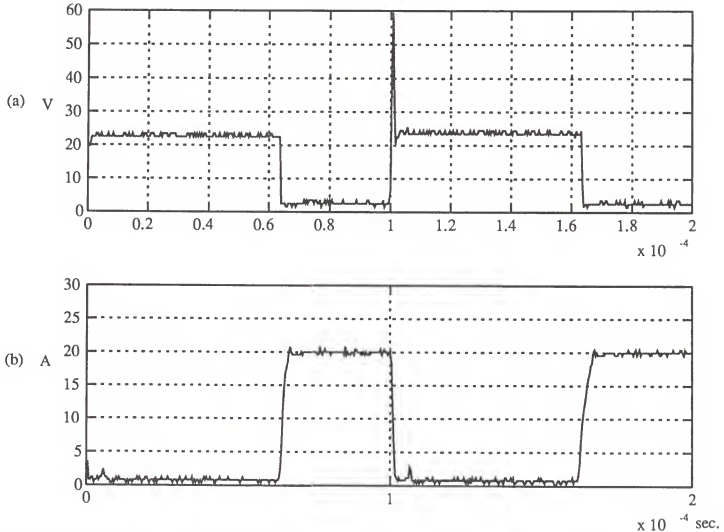


Figure 5.17. The voltage across the collector and emitter of S_{1a} (a) and the current through S_{1a} (b).

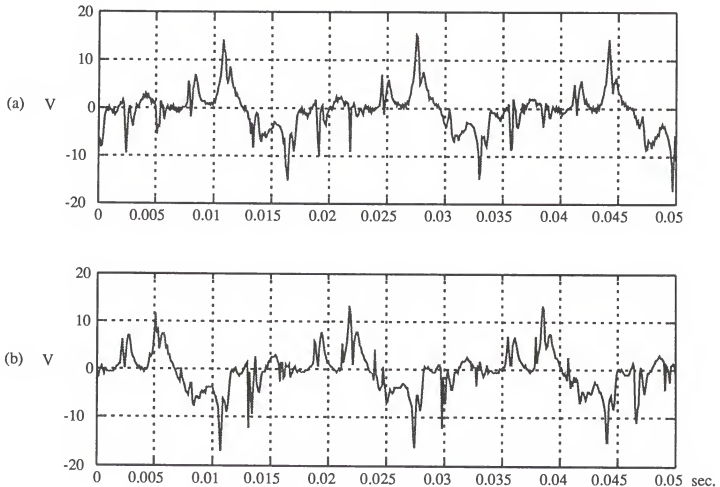


Figure 5.18. The voltage across the inverter capacitor: phase A (a) and phase (b).

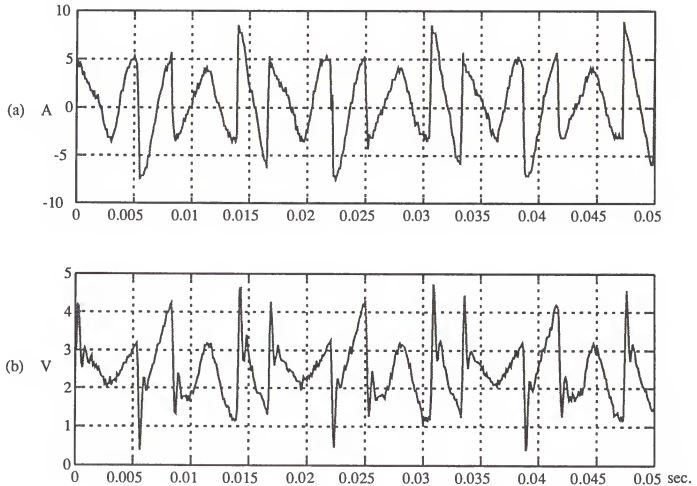


Figure 5.19. The passive filter current i_p (a) and the duty ratio reference $d_{1a}(t)$ (b).

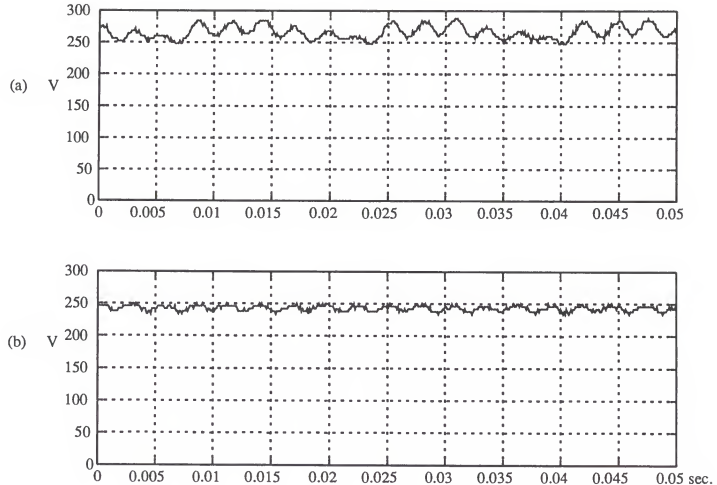


Figure 5.20. The rectifier voltage with (a) and without (b) the hybrid active/passive filter.

CHAPTER 6
SUMMARY AND CONCLUSION

It has been known that an active filter in series with a passive filter connected to the load point (known as the point of common coupling (PCC) in the power distribution industry) can ideally absorb all harmonic currents generated by the load to keep the line current and load voltage free of harmonic distortion. Voltage-fed inverters have been extensively investigated and well documented for the role of active filter .

This study investigated the feasibility of a current-fed inverter as the active filter and found out that, in series with the popular 5th-7th-11th series resonant passive filter, the current-fed inverter would have high conduction losses. Hence, it is an impractical application. The losses are greatly reduced if the current-fed inverter is in series with a passive filter that is parallel-resonated at the fundamental frequency. The VA ratings of the semiconductor switches in the inverter are low in this case, too.

This parallel-resonant passive filter reduces the overall losses in the hybrid active/passive filter whether or not a voltage-fed or current-fed inverter is employed for the role of active filter. However, the current-fed inverter has the advantage of simplicity in control and does not interfere with the dynamics of the power system being filtered. A simple open-loop control circuit consisting of only current sensors and operational amplifiers can provide the essential duty ratios for the current-fed inverter to perform active filtering.

The duty ratios and control algorithm for the 3ϕ current-fed active filtering have been derived and checked with simulations and an experiment. The experiment of active filtering of a prototype 3ϕ one-branch power distribution system loaded with a full-bridge rectifier of 3kW output has been done with a current-fed inverter in series with a parallel-resonant passive filter connected to the load point. The experimental results agreed with simulation, and the correctness of the analysis done in this dissertation has been proven.

In conclusion, the experiment with the prototype system has proven that the current-fed inverter is well suited for active filtering if a parallel-resonant passive filter tuned at the fundamental frequency is in series with it. This hybrid filter has a low overall loss compared to the configuration the 5th-7th-11th series-resonant filter. By nature the low rating semiconductor devices have low conduction losses, and the total losses in the hybrid filter can be minimized by choosing the right specifications for the passive filter and semiconductor components. Although the parallel-resonant passive filter in series with a voltage-fed inverter will have the lowest overall losses, the current-fed hybrid filter can operate smoothly without a complicated feedback control loop which is necessary for the voltage-fed inverter to function correctly. The disadvantage of this configuration is that, for the same capacitance in both types of passive filters, the VA ratings of the parallel-resonant filter are two times of the ratings of the compound series-resonant filter. Because the parallel-resonant inductor has the same VA rating as the capacitor and the inductor VA ratings in the compound series-resonant filters are very low compared to the rating of the capacitor. However, since the loss in the inverter is always low and does not vary much with the capacitance changes of the parallel-resonant filter, the proposed hybrid filter has more design flexibility over the conventional type of hybrid filter.

APPENDIX A
PSpice® FILES

A.1. Circuit File for Figures 1.1(a) and 1.3

* v_s: V(1000);
* i_s: i(Las);
* i_{s1}: fundamental component of is.

```
01/09/95: Model0.cir Bare Behavior Study
.PARAM Lf={46.91m}, Cf={150u}, Cinv={100u}
.PARAM RLf={0.884}, RCf={0.0884}, Rload={16}
Vas    1000    0    SIN(0V 169.70V 60Hz 0 0 0)
Vbs    2000    0    SIN(0V 169.70V 60Hz 0 0 -120)
Vcs    3000    0    SIN(0V 169.70V 60Hz 0 0 -240)

Las    1000    1010    1.32mH
Ras    1010    1020    0.265ohm
Lbs    2000    2010    1.32mH
Rbs    2010    2020    0.265ohm
Lcs    3000    3010    1.32mH
Rcs    3010    3020    0.265ohm

Vta    1020    1030    0V
Vtb    2020    2030    0V
Vtc    3020    3030    0V

Xload  1030    2030    3030    RECTIFIER

*
.SUBCKT RECTIFIER 110   120    130
Lx     100     105     5mH
Cx     105     200     150uF
Rx     105     200     {Rload}
D11    110     100     DX
D12    200     110     DX
D21    120     100     DX
D22    200     120     DX
D31    130     100     DX
```

```
D32    200    130    DX
.MODEL DX D(Is=1e-4A, N=1.0)
.ENDS
*
.TRAN 50us 200mS 0mS 20uS UIC
.FOUR 60Hz 15 i(Las) V(1020)
;.PROBE
.END
```

A.2. Circuit File for Figure 1.1(a)

```
* E1 will have a modulated 60Hz sinewave

To generate sgas and surges
V1     10     0      SIN(0V 1V 60Hz 0 0 0)
V2     20     0      SIN(0V 1V 2Hz 0 0 )
E1     30     0      VALUE={V(10)*V(20)}
.TRAN 50uS 200mS 0mS 25uS UIC
.PROBE
.END
```

A.3. Circuit File for Figure 2.5: Phas-Shifted Square-Wave Drive

* v_{AN}: V(110)
* v_{BN}: V(120)
* v_{AB}: V(110,120)

```
PHASE-SHIFTED SQUARE-WAVE DRIVE
Vin   100  0     10V
S11   100  110  200   0     VSW
S12   110  0     0     200   VSW
S21   100  120  210   0     VSW
S22   120  0     0     210   VSW
Vs1   200   0     PULSE(-10V 10V 0mS 0.1mS 0.1mS 4.9mS 10mS)
Vs2   210   0     PULSE(-10V 10V 4mS 0.1mS 0.1mS 4.9mS 10mS)
.MODEL VSW VSWITCH(Ron=0.1ohm, Roff=1e6ohm, Von=1V, Voff=0V)
.TRAN 0.1mS 200mS 0mS 0.1mS UIC
.FOUR 100Hz V(110,120)
.PROBE
.END
```

A.4. Circuit File for Figures 2.8, 2.9(c), 2.10(a), and 2.11(a): HPWM Inverter

* v_{AB}: V(110,120)
* V(250) is the carrier function, it can be changed from the ramp formation to the triangular formatiom

```
DC-AC CONVERTER [HPWM, fo=60Hz mf=15 ma=0.8]
Vdc   100   0     100V
;
S11   100   110   200   0     VSW
S12   110   0     210   0     VSW
S21   100   120   220   0     VSW
S22   120   0     230   0     VSW
;
Vtri  250   0     PULSE(0V 10V 0uS 0.555555ms 0.555555mS 0.1uS 1.111111mS)
Vref  350   0     SIN(0V 8.0V 60Hz 0 0 0)
Eabs  360   0     VALUE={ABS(V(350))}
;
Gx1   0     230   350   0     10
Dx1   230   231   Dx
Vx1   231   0     15V
Dx2   232   230   Dx
Vx2   232   0     -15V
;
Gx2   0     220   0     350   10
DX3   220   221   Dx
Vx3   221   0     15V
Dx4   222   220   Dx
Vx4   222   0     -15V
;
Gx3   0     420   350   0     10
Dx5   420   421   Dx
Vx5   421   0     15V
Dx6   422   420   Dx
Vx6   422   0     -15V
;
Gpwm  0     430   360   250   10
Dx7   430   431   Dx
Vx7   431   0     15V
Dx8   432   430   Dx
Vx8   432   0     -15V
;
Rdr1  200   0     100ohm
Sa1   200   201   420   0     VSW
Sb1   201   202   430   0     VSW
```

```
Vs1   202   0     15V
Sc1   200   203   0     420   VSW
Sd1   203   204   0     430   VSW
Vs2   204   0     15V
;
Rdr2  210   0     100ohm
Sa2   210   211   420   0     VSW
Sb2   211   212   0     430   VSW
Vs3   212   0     15V
Sc2   210   213   0     420   VSW
Sd2   213   214   430   0     VSW
Vs4   214   0     15V
;
.MODEL VSW VSWITCH(Ron=0.1ohm Roff=1E5ohm Von=2.5V Voff=0V)
.MODEL DX D(Is=1E-6A N=0.25)
.OPTION ITL4=1000000 ITL5=0 RELTOL=0.01 ABSTOL=100uA VNTOL=2.5mV
.TRAN 5uS 0.05S 0.0S 5uS
.FOUR 60 50 V(110,120)
.print TRAN V(110,120)
.probe
.END
```

A.5. Circuit File for Figures 2.9(a) and 2.12: BPWM Inverter

* v_{AB}: V(110,120)

```
DC-AC CONVERTER [Biploar PWM, fo=60Hz mf=17 ma=0.8]
Vdc   100   0     100V
;
S11   100   110   200   0     VSW
S12   110   0     210   0     VSW
S21   100   120   210   0     VSW
S22   120   0     200   0     VSW
;
Vtri  250   0     PULSE(10V -10V 0uS 0.490196mS 0.490196mS 0.1568nS
+                 980.3921568uS)
Vref  350   0     SIN(0V 8.0V 60Hz 0.245098mS 0 0)
;
Gx1   0     200   350   250   10
Dx1   200   201   Dx
Vx1   201   0     15V
Dx2   202   200   Dx
Vx2   202   0     -15V
;
Gx2   0     210   250   350   10
DX3   210   211   Dx
Vx3   211   0     15V
Dx4   212   210   Dx
Vx4   212   0     -15V
;
.MODEL VSW VSWITCH(Ron=0.1ohm Roff=1E5ohm Von=1.5V Voff=0V)
.MODEL DX D(Is=1E-6A N=0.25)
.OPTION ITL4=1000000 ITL5=0 RELTOL=0.01 ABSTOL=100uA VNTOL=2.5mV
.TRAN 5uS 0.05S 0S 5uS
;.FOUR 60 50 V(110,120)
.PRINT TRAN V(110,120)
.PROBE
.END
```

A.6. Circuit File for Figure 2.9(b), 2.10(b), and 2.11(b): UPWM Inverter

* v_{AB}: V(110,120)
* V(250) is the carrier function, it can be changed from the ramp formation to the triangular formatiom

```
DC-AC CONVERTER [UNIPOLAR PWM, fo=60Hz mf=9 ma=0.8, triangular]
Vdc    100    0      100V
;
S11    100    110    200    0      VSW
S12    110    0      210    0      VSW
S21    100    120    220    0      VSW
S22    120    0      230    0      VSW
;
Vtri   250    0      PULSE(10V -10V 0uS 0.9259259255mS 0.9259259255mS 0.85pS
1851.851851uS)
Vref+  350    0      SIN(0V 8.0V 60Hz  0.46296296275mS 0  0)
Vfre-  360    0      SIN(0V 8V 60Hz 0.46296296275mS  0 180)
;
Gx1    0      230    250    360    10
Dx1    230    231    Dx
Vx1    231    0      15V
Dx2    232    230    Dx
Vx2    232    0      -15V
;
Gx2    0      220    360    250    10
DX3    220    221    Dx
Vx3    221    0      15V
Dx4    222    220    Dx
Vx4    222    0      -15V
;
Gx3    0      200    350    250    10
Dx5    200    201    Dx
Vx5    201    0      15V
Dx6    202    200    Dx
Vx6    202    0      -15V
;
Gpwm   0      210    250    350    10
Dx7    210    211    Dx
Vx7    211    0      15V
Dx8    212    210    Dx
Vx8    212    0      -15V
;
.MODEL VSW VSWITCH(Ron=0.1ohm Roff=1E5ohm Von=1.5V Voff=0V)
.MODEL DX D(Is=1E-6A N=0.25)
```

```
.OPTION ITL4=1000000 ITL5=0 RELTOL=0.01 ABSTOL=100uA VNTOL=2.5mV
.TRAN 5uS 0.0504629629275S 0.4629629275mS 5uS
;.FOUR 60 50 V(110,120)
.PRINT TRAN V(110,120)
.PROBE
.END
```

A.7.Circuit File for Figure 2.16: 3ϕ Voltage-Fed Inverter

* v_a, v_b, and v_c: V(200,500), V(300,500), and V(400,500)
* d_a: AC part of V(800)
* v_{AB}: V(200,300)

```
Three-Phase Voltage-Fed Inverter
Vdc     100     0       100V

Sa1     100     110     710     0       VSW
Da1     110     100     DX
Sa2     110     0       0       710     VSW
Da2     0       110     DX

Sb1     100     120     730     0       VSW
Db1     120     100     DX
Sb2     120     0       0       730     VSW
Db2     0       120     DX

Sc1     100     130     750     0       VSW
Dc1     130     100     DX
Sc2     130     0       0       750     VSW
Dc2     0       130     DX

La      110     200     1mH
Lb      120     300     1mH
Lc      130     400     1mH
Ca      200     500     50uF
Cb      300     500     50uF
Cc      400     500     50uF
Ra      200     50      0.01Kohm
Rb      300     50      0.01Kohm
Rc      400     50      0.01Kohm

Rg      500     0       10e6ohm

Vxda    800     0       SIN(5V 4V 200Hz 0 0 0)
Vxdb    810     0       SIN(5V 4V 200Hz 0 0 -120)
Vxdc    820     0       SIN(5V 4V 200Hz 0 0 -240)

Vpulse  830     0       PULSE(0V 10V 0uS 99.5uS 99.5us 0.5uS
200uS)

Xa1     800     830     710     BUFFER
Xb1     810     830     730     BUFFER
```

```
Xc1          820          830          750          BUFFER

.SUBCKT BUFFER100         200          30
Gx           0            10           100          200          5
Dx1          10           20           DXX
V1           20           0            15V
Dx2          21           10           DXX
V2           21           0            -15V
Rx           10           30           1Kohm
Cx           30           0            0.2nF
.MODEL DXX D(IS=100E-6A, Vj=0.5V, N=1)
.ENDS

.MODEL VSW VSWITCH(Ron=0.1ohm Roff=50E3ohm Von=2V Voff=1V)
.MODEL DX D(Is=100E-6A Vj=0.75V  N=1)

.OPTION  ITL4=200 ABSTOL=5.uA VNTOL=1mV
+                NOMOD NOBIAS NOECHO

.TRAN 10us 150mS 0mS 2uS UIC
.PROBE
.END
```

A.8. Circuit File for Figure 2.20: 3f Current-Fed Inverter

```
* va, vb, and vc: V(410,440), V(420,440), and V(430,440)
* v'a, v'b, and v'c: V(415,450), V(425,450), and V(435,450)
* da: V(100)
* iL: i(Ldc)

Current-fed Inverter
Vdc   401   0     100V
Ldc   401   400   5mH
;
Sa1   400   412   800   0     VSWI
Da1   412   410   DX
Da2   410   414   DX
Sa2   414   0     810   0     VSWI
;
Sb1   400   422   825   0     VSWI
Db1   422   420   DX
Db2   420   424   DX
Sb2   424   0     835   0     VSWI
;
Sc1   400   432   845   0     VSWI
Dc1   432   430   DX
Dc2   430   434   DX
Sc2   434   0     855   0     VSWI

Cia   410   440   100uF
Cib   420   440   100uF
Cic   430   440   100uF
Rg          440         0          10E6ohm

La          410         415        1mH
Lb          420         425        1mH
Lc          430         435        1mH
Ca          415         450        50uF
Cb          425         450        50uF
Cc          435         450        50uF
Ra          415         450        10ohm
Rb          425         450        10ohm
Rc          435         450        10ohm

Viref+ 930  0    PULSE(0V 10V 0uS 198uS 1uS 0.5uS 200uS)
Viref- 940  0    PULSE(0V 10V 100uS 198uS 1uS 0.5uS 200uS)

Vda         100         0          SIN(0V 3V 200Hz 0 0 0)
```

```
Vdb          200          0            SIN(0V 3V 200Hz 0 0 -120)

Ea+          700          0            VALUE={(10/3)+V(100)}
Eb+          710          700          VALUE={(10/3)+V(200)}
Vc+          720          0            10V


Ea-          730          0            VALUE={(10/3)-V(100)}
Eb-          740          730          VALUE={(10/3)-V(200)}
Vc-          750          0            10V


Xa1   700    930          800          BUFFER
Xb1x         710          930          820          BUFFER
Xc1x         720          930          840          BUFFER
Xa2          730          940          810          BUFFER
Xb2x         740          940          830          BUFFER
Xc2x         750          940          850          BUFFER
Eb1          825          0            VALUE={V(820)-V(800)}
Ec1          845          0            VALUE={V(840)-V(820)}
Eb2          835          0            VALUE={V(830)-V(810)}
Ec2          855          0            VALUE={V(850)-V(830)}

.SUBCKT BUFFER100    200          30
Gx           0            10           100          200          5
Dx1          10           20           DXX
V1           20           0            15V
Dx2          21           10           DXX
V2           21           0            0V
Rx           10           30           1Kohm
Cx           30           0            0.2nF
.MODEL DXX D(IS=100E-6A, Vj=0.5V, N=1)
.ENDS

.MODEL VSWI VSWITCH(Ron=0.1ohm Roff=15E3ohm Von=5V Voff=0.2V)
.MODEL DX D(Is=100E-6A Vj=0.75V  N=1)
.OPTION  ITL4=200 RELTOL=0.01 ABSTOL=5.uA VNTOL=1mV
+              NOMOD NOBIAS NOECHO

.TRAN 10us 50mS 0mS 2uS UIC
.PROBE
.END
```

A.9. Circuit File for Figure 4.6: Active Filtering with Hybrid Current-Fed Active/LC Parallel Passive Filter

```
* i_as= i(Las)
* i_aL= i(Vta)
* i_ap= i(Via)
* i_aCp= i(Xpfa.Cf)
* i_aLp= i(Xpfa.Lf)
* i_dc= i(Ldc)
* i_load= i(xload.Lx)
* v_aCi= V(1040)
* v_aL= V(1020)
* v_pn= V(xload.100,xload.200)
*
CURRENT_FED ACTIVE FILTERING
.PARAM Lf={46.91m}, Cf={150u}, Cinv={100u}
.PARAM RLf={0.884}, RCf={0.0884}, Rload={10}
Vas   1000   0    SIN(0V 208V 60Hz 0 0 0)
Vbs   2000   0    SIN(0V 208V 60Hz 0 0 -120)
Vcs   3000   0    SIN(0V 208V 60Hz 0 0 -240)

Las   1000   1010  4.572mH
Ras   1010   1020  0.7372ohm
Lbs   2000   2010  4.572mH
Rbs   2010   2020  0.7372ohm
Lcs   3000   3010  4.572mH
Rcs   3010   3020  0.7372ohm

Vta   1020   1030  0V
Vtb   2020   2030  0V
Vtc   3020   3030  0V

Xload  1030   2030   3030   RECTIFIER

Xpfa   1020   1040   P_FILTER
Xpfb   2020   2040   P_FILTER
Xpfc   3020   3040   P_FILTER
*
.SUBCKT RECTIFIER 110  120   130
Lx     100    105    10mH
Cx     105    200    50uF
Rx     105    200    {Rload}
D11    110    100    DX
```

```
D12   200   110   DX
D21   120   100   DX
D22   200   120   DX
D31   130   100   DX
D32   200   130   DX
.MODEL DX D(Is=1e-4A, N=1.0)
.ENDS
*
.SUBCKT P_FILTER      100   200
RLf   100   101   {RLf}
Lf    101   200   {Lf}
RCf   100   102   {RCf}
CF    102   200   {Cf}
.ENDS
*
* Reference Operation
*
Eiar  100   0     VALUE={i(Vta)}
Eibr  200   0     VALUE={i(Vtb)}
Eicr  300   0     VALUE={i(Vtc)}
Xia   100   110   BIQUAD
Xib   200   210   BIQUAD
Xic   300   310   BIQUAD

Era   120   0     VALUE={V(100)-V(110)+3*(-i(Vas)-V(110))}
Erb   220   0     VALUE={V(200)-V(210)+3*(-i(Vbs)-V(210))}
Erc   320   0     VALUE={V(300)-V(310)+3*(-i(Vcs)-V(310))}
Xha   120   130   4TH
Xhb   220   230   4TH
Xhc   320   330   4TH
*
.SUBCKT BIQUAD  10    100 PARAMS: R1=26Kohm, C1=0.1uF, R2=27.6Kohm
R1    10    20    {R1}
R2    20    30    {R1}
C1    20    30    {C1}
R3    30    40    {R1}
C2    40    50    {C1}
R4    50    60    10Kohm
R5    60    70    10Kohm
R6    70    20    {R1}

R7    70    90    10Kohm
R8    90    100   10Kohm
Rx    70    80    {R2}
Cx    80    0     0.1uF
```

```
Xop1  0    20    30    OP_IDEAL
Xop2  0    40    50    OP_IDEAL
Xop3  0    60    70    OP_IDEAL
Xop4  80   90    100   OP_IDEAL
.ENDS
*
.SUBCKT 4TH    10    140
R1    10    20    9.5Kohm
R2    20    30    3.6Kohm
C1    20    30    0.01uF
R3    30    40    6.6Kohm
C2    40    50    0.01uF
R4    50    60    10Kohm
R5    60    70    10Kohm
R6    70    20    6.6Kohm

R7    30    80    15Kohm
R8    10    80    10Kohm
R9    70    80    15Kohm
R10   80    90    10Kohm

R11   90    100   6.6Kohm
R12   100   110   6.6Kohm
C3    110   0     4nF
C4    100   120   26nF
Xop   110   120   120   OP_IDEAL

R13   120   130   5.5Kohm
R14   130   140   10.Kohm
Xopp  0     130   140   OP_IDEAL


Xop1  0    20    30    OP_IDEAL
Xop2  0    40    50    OP_IDEAL
Xop3  0    60    70    OP_IDEAL
Xop4  0    80    90    OP_IDEAL
.ENDS


.SUBCKT OP_IDEAL 10    20    30
Ri    10    20    2e6ohm
Egain 31    0     10    20    2e3
Ro    31    30    1ohm
.ENDS
*
* Current Inverter Part
```

```
*
Vdc   401   0    PULSE(0V 8.4V 20mS 1mS 2mS 10S 20S)
Ldc   401   400   10mH
;
Sa1   400   412   800   0    VSWI
Da1   412   410   DX
Da2   410   414   DX
Sa2   414   0    810   0    VSWI
;
Sb1   400   422   825   0    VSWI
Db1   422   420   DX
Db2   420   424   DX
Sb2   424   0    835   0    VSWI
;
Sc1   400   432   845   0    VSWI
Dc1   432   430   DX
Dc2   430   434   DX
Sc2   434   0    855   0    VSWI
;
Liap  1040  1050  .1H
Libp  2040  2050  .1H
Licp  3040  3050  .1H
Via   1050  0     0V
Vib   2050  0     0V
Vic   3050  0     0V

Lias  410   440   .1H
Libs  420   440   .1H
Lics  430   440   .1H
;
Ka    Liap  Lias  0.999999
Kb    Libp  Libs  0.999999
Kc    Licp  Lics  0.999999
;
Cia   410   440   {Cinv}
Cib   420   440   {Cinv}
Cic   430   440   {Cinv}

;
Viref+ 930   0     PULSE(0V 10V 20mS 123uS 1uS 1uS 125uS)
;Viref- 940   0     PULSE(0V 10V 50uS 98uS 1uS 1uS 100uS)
Vaf   60    0    PULSE(0V 1.V 16.666mS 1mS 1mS 10S 20S)
;

Ea+   700   0     VALUE={V(60)*((10/3)+V(130)/5.4)}
Eb+   710   700   VALUE={V(60)*((10/3)+V(230)/5.4)}
```

```
;Ec+   720   710   VALUE={V(60)*((10/3)+V(330)/5.4)}
Vc+   720   0     10V
;
Ea-   730   0     VALUE={V(60)*((10/3)-V(130)/5.4)}
Eb-   740   730   VALUE={V(60)*((10/3)-V(230)/5.4)}
;Ec-   750   740   VALUE={V(60)*((10/3)-V(330)/5.4)}
Vc-   750   0     10V
;
Xa1   700   930   800   BUFFER
Xb1x  710   930   820   BUFFER
Xc1x  720   930   840   BUFFER
Xa2   730   930   810   BUFFER
Xb2x  740   930   830   BUFFER
Xc2x  750   930   850   BUFFER
Eb1   825   0     VALUE={V(820)-V(800)}
Ec1   845   0     VALUE={V(840)-V(820)}
Eb2   835   0     VALUE={V(830)-V(810)}
Ec2   855   0     VALUE={V(850)-V(830)}

.SUBCKT BUFFER 100   200   30
Gx    0     10    100   200   5
Dx1   10    20    DXX
V1    20    0     15V
Dx2   21    10    DXX
V2    21    0     0V
Rx    10    30    1Kohm
Cx    30    0     2nF
.MODEL DXX D(IS=100E-6A, Vj=0.5V, N=1)
.ENDS
.MODEL VSWI VSWITCH(Ron=0.1ohm Roff=15E3ohm Von=5V Voff=0.2V)
.MODEL DX D(Is=100E-6A Vj=0.75V  N=1)
.OPTION  ITL4=200 RELTOL=0.01 PIVREL=1E-3 PIVTOL=1E-13 ABSTOL=1.uA
+       VNTOL=1mV NOMOD NOBIAS NOEC.TRAN 5uS 300ms 0ms 1.2uS UIC
.FOUR 60Hz 25 V(1020) V(2020) V(3020) i(Las) i(Lbs) i(Lcs)
.PROBE          V(1000) V(2000) V(3000)  V(1020) V(2020) V(3020)
+               V(100) V(200) V(300) V(120) V(220) V(320)
;   V(800) V(810)  V(820)  V(830)  V(840)  V(850)   V(825)  V(835)  V(845) V(855)
+               V(410)    V(420)     V(430) V(700)  V(710)  V(730)
+               V(740) V(412,410) V(400,401) V(401,412) V(401)
+       i(Ldc) i(Vta) i(Vtb) i(Vtc)
+               i(Cia) i(Cib) i(Cic) i(Las) i(Lbs) i(Lcs) V(930)
+               V(Xload.100,Xload.200) V(401) i(Xpfa.Lf) i(Xpfb.Lf) i(Xpfc.Lf)
+               i(Xpfa.Cf) i(Xpfb.Cf) i(Xpfc.Cf) i(Sa1) i(Sa2) i(Sb1) i(Sb2) i(Sc1) i(Sc2)
+               V(130) V(230) V(330) i(xload.Lx) V(xload.100,xload.200)
+               V(xload.105,xload.200)
.END
```

A.10. Circuit File for Figure 4.7: 3ϕ Rectifier without Any Filtering

```
* i_as= i(Las)
* i_load= i(xload.Lx)
* v_aL= V(1020)
* v_pn= V(xload.100,xload.200)
*
01/09/95: Model0.cir Bare Behavior Study
.PARAM Rload={10}
Vas   1000   0   SIN(0V 208.0V 60Hz 0 0 0)
Vbs   2000   0   SIN(0V 208.0V 60Hz 0 0 -120)
Vcs   3000   0   SIN(0V 208.0V 60Hz 0 0 -240)

Las   1000   1010  4.572mH
Ras   1010   1020  0.7372ohm
Lbs   2000   2010  4.572mH
Rbs   2010   2020  0.7372ohm
Lcs   3000   3010  4.572mH
Rcs   3010   3020  0.7372ohm

Vta   1020   1030  0V
Vtb   2020   2030  0V
Vtc   3020   3030  0V

Xload  1030   2030   3030   RECTIFIER

*
.SUBCKT RECTIFIER 110   120    130
Lx    100    105    10mH
Cx    105    200    50uF
Rx    105    200    {Rload}
D11   110    100    DX
D12   200    110    DX
D21   120    100    DX
D22   200    120    DX
D31   130    100    DX
D32   200    130    DX
.MODEL DX D(Is=1e-4A, N=1.0)
.ENDS
.OPTION  ITL4=200 RELTOL=0.01 PIVREL=1E-3 PIVTOL=1E-13 ABSTOL=1.uA
+        VNTOL=1mV NOMOD NOBIAS NOECHO
.TRAN 50us 200mS 0mS 10uS UIC
.FOUR 60Hz 15 i(Las) V(1020)
.PROBE
.END
```

A.11. Circuit File for Figure 4.9: Active Filtering with Hybrid Voltage-Fed Active/LC Parallel Passive Filter

```
* ia= i(Liav)
* ias= i(Las)
* iaL= i(Vta)
* iap= i(Via)
* iaCp= i(C1pax)
* iaLp= i(L1pax)
* iload= i(xr3x.Lx)
* vaCi= V(1593)
* vaL= V(1520)
* vpn= V(xr3x.100,xr3x.200)
*
Volt-Fed Compensation
;
; Lf=passive parallel filter inductance
; Cf=filter capacitance
; Rlf, Rcf resistance of Lf & Cf
; IL= DC current of the inverter
; d1 - d23: harmonic duty ratios of the inverter
; tha1 - tha23: phase angles
;
.PARAM Lf={46.91e-3}, Cf={150e-6}, Cinv={200e-6} Linv={0.1e-3}
.PARAM Rlf={0.884}, Rcf={0.0884} ,Vdc={62}
;
.PARAM d1={0.00384496}, d5={3.50876}, d7={1.43662}, d11={0.306114}
.PARAM d13={0.0896344}, d17={0.138073}, d19={0.20096}, d23={0.281585}
d25={0.308038}
;
.PARAM ta1={-70.6914}, ta5={12.964}, ta7={-5.25809}, ta11={112.968}
.PARAM ta13={92.0879}, ta17={17.3968}, ta19={-9.14031}, ta23={112.84}
ta25={84.3423}
;
.PARAM tb1={ta1-120}, tb5={ta5+120} tb7={ta7-120}, tb11={ta11+120}
.PARAM tb13={ta13-120},tb17={ta17+120},tb19={ta19-120},tb23={ta23+120}
tb25={ta25-120}
;
.PARAM tc1={ta1+120}, tc5={ta5-120} tc7={ta7+120}, tc11={ta11-120}
.PARAM tc13={ta13+120},tc17={ta17-120},tc19={ta19+120},tc23={ta23-120}
tc25={ta25+120}
;
Vax    1500   0      SIN(0V 208V 60Hz 0 0 0)
```

```
Vbx    2500   0      SIN(0V 208V 60Hz 0 0 -120)
Vcx    3500   0      SIN(0V 208V 60Hz 0 0 -240)
;
La1x   1500   1510   4.572mH
Ra1x   1510   1520   0.7372ohm
;
Lb1x   2500   2510   4.572mH
Rb1x   2510   2520   0.7372ohm
;
Lc1x   3500   3510   4.572mH
Rc1x   3510   3520   0.7372ohm
;
Rthax  1520   1590   0.01ohm
R1pax  1590   1591   {Rlf}
L1pax  1591   1593   {Lf}
R1esax 1590   1592   {Rcf}
C1pax  1592   1593   {Cf}
;
Liap   1593   1594   0.1H
Via    1594   0      0.0V
;
Rthbx  2520   2590   0.01ohm
R1pbx  2590   2591   {Rlf}
L1pbx  2591   2593   {Lf}
R1esbx 2590   2592   {Rcf}
C1pbx  2592   2593   {Cf}
;
Libp   2593   2594   0.1H
Vib    2594   0      0.0V
;
Rthcx  3520   3590   0.01ohm
R1pcx  3590   3591   {Rlf}
L1pcx  3591   3593   {Lf}
R1escx 3590   3592   {Rcf}
C1pcx  3592   3593   {Cf}
;
Licp   3593   3594   0.1H
Vic    3594   0      0.0V
;
Vta3x  1590   1600   0V
Vtb3x  2590   2600   0V
Vtc3x  3590   3600   0V
;
Xr3x   1600   2600   3600      RECTIFIER
;
.SUBCKT RECTIFIER 110    120    130
```

```
Lx          100          101          10mH
Cx   101    200   50uF
Rx   101    200   10ohm
D11  110    100   DX
D12  200    110   DX
D21  120    100   DX
D22  200    120   DX
D31  130    100   DX
D32  200    130   DX
.MODEL DX D(Is=1E-4A N=1.0)
.ENDS
;
Vdc          400          0          PULSE(0V {Vdc} 0mS 1mS 1mS 10S 20S)
;
Sa1  400    410   800   0    VSWI
Da1  410    400   DX
Da2  0      410   DX
Sa2  410    0     0   800    VSWI
;
Sb1  400    420   820   0    VSWI
Db1  420    400   DX
Db2  0      420   DX
Sb2  420    0     0   820    VSWI
;
Sc1  400    430   840   0    VSWI
Dc1  430    400   DX
Dc2  0      430   DX
Sc2  430    0     0   840    VSWI
;
Lias 411    440   0.1H
Libs 421    440   0.1H
Lics 431    440   0.1H
;
Ka   Liap   Lias  0.9999999
Kb   Libp   Libs  0.9999999
Kc   Licp   Lics  0.9999999
;
Liav         410          411          {Linv}
Libv         420          421          {Linv}
Licv         430          431          {Linv}
Cia  411    440   {Cinv}
Cib  421    440   {Cinv}
Cic  431    440   {Cinv}
;
Vda1 900    901   SIN(0V {d1} 60Hz 0 0 {ta1})
Vda5 901    902   SIN(0V {d5} 300Hz 0 0 {ta5})
```

```
Vda7   902   903   SIN(0V {d7} 420Hz 0 0 {ta7})
Vda11  903   904   SIN(0V {d11} 660Hz 0 0 {ta11})
Vda13  904   905   SIN(0V {d13} 780Hz 0 0 {ta13})
Vda17  905   906   SIN(0V {d17} 1020Hz 0 0 {ta17})
Vda19  906   907   SIN(0V {d19} 1140Hz 0 0 {ta19})
Vda23  907   908   SIN(0V {d23} 1380Hz 0 0 {ta23})
Vda25  908   0     SIN(0V {d25} 1500Hz 0 0 {ta25})
;
Vdb1   910   911   SIN(0V {d1} 60Hz 0 0 {tb1})
Vdb5   911   912   SIN(0V {d5} 300Hz 0 0 {tb5})
Vdb7   912   913   SIN(0V {d7} 420Hz 0 0 {tb7})
Vdb11  913   914   SIN(0V {d11} 660Hz 0 0 {tb11})
Vdb13  914   915   SIN(0V {d13} 780Hz 0 0 {tb13})
Vdb17  915   916   SIN(0V {d17} 1020Hz 0 0 {tb17})
Vdb19  916   917   SIN(0V {d19} 1140Hz 0 0 {tb19})
Vdb23  917   918   SIN(0V {d23} 1380Hz 0 0 {tb23})
Vdb25  918   0     SIN(0V {d25} 1500Hz 0 0 {tb25})
;
Vdc1   920   921   SIN(0V {d1} 60Hz 0 0 {tc1})
Vdc5   921   922   SIN(0V {d5} 300Hz 0 0 {tc5})
Vdc7   922   923   SIN(0V {d7} 420Hz 0 0 {tc7})
Vdc11  923   924   SIN(0V {d11} 660Hz 0 0 {tc11})
Vdc13  924   925   SIN(0V {d13} 780Hz 0 0 {tc13})
Vdc17  925   926   SIN(0V {d17} 1020Hz 0 0 {tc17})
Vdc19  926   927   SIN(0V {d19} 1140Hz 0 0 {tc19})
Vdc23  927   928   SIN(0V {d23} 1380Hz 0 0 {tc23})
Vdc25  928   0     SIN(0V {d25} 1500Hz 0 0 {tc25})
;
Viref+ 930   0     PULSE(0V 10V 0uS 123uS 1uS 1uS 125uS)
;
Ea+    700   0     VALUE={5+V(900,0)}
Eb+    710   0     VALUE={5+V(910,0)}
Ec+    720   0     VALUE={5+V(920,0)}
;
Xa1            700          930          800          BUFFER
Xb1            710          930          820          BUFFER
Xc1            720          930          840          BUFFER

.SUBCKT BUFFER100          200          30
Gx             0            10           100          200          5
Dx1            10           20           DXX
V1             20           0            15V
Dx2            21           10           DXX
V2             21           0            -15V
Rx             10           30           1Kohm
Cx             30           0            1nF
```

```
.MODEL DXX D(IS=100E-6A, Vj=0.5V, N=1)
.ENDS

;
.MODEL VSWI VSWITCH(Ron=0.1ohm Roff=15E3ohm Von=5V Voff=0V)
.MODEL DX D(Is=100E-6A Vj=0.5V N=1)
.OPTIONS ITL4=2000 ITL5=0 PIVREL=1E-3 PIVTOL=1E-13 ABSTOL=5uA
VNTOL=1mV NUMDGT=8
+               RELTOL=0.01
.TRAN 10uS 150mS 0mS 1.25uS UIC
;.PRINT TRAN V(1520) I(La1x)
.FOUR 60Hz 25 V(1520) I(La1x)
.PROBE i(La1x) i(Lb1x) i(lc1x) V(1520) V(2520) V(3520) V(1593) V(2593) V(3593)
+               i(Vta3x) i(Vtb3x) i(Vtc3x) i(Cia) i(Cib) i(Cic) i(Via) i(Vib) i(Vic)
+               V(900) V(910) V(700) V(710) i(Sa1) i(Sb1) i(Sc1) i(L1pax) i(C1pax)
+               i(Liav) i(Libv) i(Licv) V(410,440) V(420,440) V(430,440)
+               V(411,440) V(421,440) V(431,440) V(xr3x.100,xr3x.200) i(xr3x.Lx)
.END
```

A.12. The Behavior Harmonic Compensation Circuit for Calculating the Load Current Harmonics

```
* The harmonic components are obtained by performing .FOUR command with desired
* current or voltage at the end of transient analysis.

Behavior Feedback Control of Active Filtering
* 10/04/95
*For the Calculation of Load Harmonic Current Components
.PARAM Lf={70.3619m}, Cf={100u}, Cinv={100u}
.PARAM RLf={1.33}, RCf={0.133}, Rload={24} Vs={169.7}
Vas   1000   0   SIN(0V {Vs} 60Hz 0 0 0)
Vbs   2000   0   SIN(0V {Vs} 60Hz 0 0 -120)
Vcs   3000   0   SIN(0V {Vs} 60Hz 0 0 -240)

Las   1000   1010  2.64mH
Ras   1010   1020  0.53ohm
Lbs   2000   2010  2.64mH
Rbs   2010   2020  0.53ohm
Lcs   3000   3010  2.64mH
Rcs   3010   3020  0.53ohm

Vta   1020   1030  0V
Vtb   2020   2030  0V
Vtc   3020   3030  0V

Xload  1030   2030   3030   RECTIFIER

Xpfa   1020   1040   P_FILTER
Xpfb   2020   2040   P_FILTER
Xpfc   3020   3040   P_FILTER

Einva  1040   0     107   0     800
Einvb  2040   0     207   0     800
Einvc  3040   0     307   0     800

sa1   1020   1021   19Kohm
Rsa2   1021   0     1Kohm
Rsb1   2020   2021   19Kohm
Rsb2   2021   0     1Kohm
Rsc1   3020   3021   19Kohm
Rsc2   3021   0     1Kohm

*DQ transform
Xdqa   1021   101    102    103    104 AC_TO_DQ
```

```
Xdqb   2021   201    202    203    204 AC_TO_DQ
Xdqc   3021   301    302    303    304 AC_TO_DQ

R1a    101    4000   36kohm
R1b    201    4000   36kohm
R1c    301    4000   36Kohm
Rq1    4000   4010   24Kohm
Xop1   0      4000   4010   OP_IDEAL
Cq     4010   4020   0.1uF
Rq2    4020   0      200Kohm

R2a    102    4030   36kohm
R2b    202    4030   36kohm
R2c    302    4030   36kohm
Rd1    4030   4040   24kohm
Xop2   0      4030   4040   OP_IDEAL
Cd     4040   4050   0.1uF
Rd2    4050   0      200Kohm

Xa1    4020   103    4050   104    105    DQ_TO_AC
Xb1    4020   203    4050   204    205    DQ_TO_AC
Xc1    4020   303    4050   304    305    DQ_TO_AC

Vramp  6      0      PULSE(0.1V 1V 100mS 10mS 1mS 2S 5S)

Ea     107    0      VALUE={V(6)*V(105)}
Eb     207    0      VALUE={V(6)*V(205)}
Ec     307    0      VALUE={V(6)*V(305)}
*
*PWM REFERENCE
Xpwmra 107    510    515    PWM_REF
Xpwmrb 207    520    525    PWM_REF
Xpwmrc 307    530    535    PWM_REF
*
.SUBCKT RECTIFIER 110   120    130
Lx     100    105    10mH
Cx     105    200    50uF
Rx     105    200    {Rload}
D11    110    100    DX
D12    200    110    DX
D21    120    100    DX
D22    200    120    DX
D31    130    100    DX
D32    200    130    DX
.MODEL DX D(Is=1e-4A, N=1.0)
.ENDS
```

```
*
.SUBCKT P_FILTER      100    200
RLf    100    101    {RLf}
Lf     101    200    {Lf}
RCf    100    102    {RCf}
CF     102    200    {Cf}
.ENDS
*
.SUBCKT AC_TO_DQ 100   122    123    117    119
*BIQUAD
R1     100    101    81Kohm
R2     101    102    81Kohm
C1     101    102    0.1uF
R3     102    103    26.5Kohm
C2     103    104    0.1uF
R4     104    105    36Kohm
R5     105    106    36Kohm
R6     106    101    26.5Kohm
*PHASE AJDUST 1
R7     106    107    24Kohm
R8     106    108    26.5Kohm
C3     108    0      0.1uF
R9     107    109    24Kohm
*PHASE AJDUST 2
R10    109    110    24Kohm
R11    109    111    26.5Kohm
C4     111    0      0.1uF
R12    110    112    24Kohm
*PHASE AJDUST 3
R13    112    113    24Kohm
R14    112    114    26.5Kohm
C5     114    0      0.1uF
R15    113    115    24Kohm
*
R16    112    116    20Kohm
R17    116    117    2Kohm
R18    115    118    20Kohm
R19    118    119    2Kohm
R20    100    120    20Kohm
R21    120    121    2Kohm

E1     122    0      VALUE={V(121)*V(117)}
E2     123    0      VALUE={V(121)*V(119)}

Xop1   0      101    102    OP_IDEAL
Xop2   0      103    104    OP_IDEAL
```

```
Xop3   0     105    106    OP_IDEAL
Xop4   108   107    109    OP_IDEAL
Xop5   111   110    112    OP_IDEAL
Xop6   114   113    115    OP_IDEAL
Xop7   0     116    117    OP_IDEAL
Xop8   0     118    119    OP_IDEAL
Xop9   0     120    121    OP_IDEAL
.ENDS
*
.SUBCKT DQ_TO_AC 100   200   300   400   500
Eq     600   0      VALUE={V(100)*V(200)}
Ed     610   0      VALUE={V(300)*V(400)}
Rqx    600   620    5Kohm
Rdx    610   620    5Kohm
Rx     620   500    50Kohm
Xopx   0     620    500    OP_IDEAL
.ENDS
*
.SUBCKT PWM_REF 100    305    308
Ecrnt  300   0      100    0      1
Rp1    300   301    5Kohm
Rp2    301   302    100Kohm
Rp3    302   303    100ohm
Cp1    303   304    0.1uF
Rp4    304   305    2.5Kohm
Rp5    306   307    5Kohm
Rp6    307   308    5Kohm

Xp1    0     301    302    OP_IDEAL
Xp2    0     304    305    OP_IDEAL
Xp3    305   306    306    OP_IDEAL
Xp4    0     307    308    OP_IDEAL
.ENDS
*
.SUBCKT OP_IDEAL 10    20     30
Ri     10    20     1e7ohm
Egain  31    0      10     20     1e4
Ro     31    30     1ohm
.ENDS
.OPTION ACCT NOMOD NOBIAS NOECHO
.TRAN 10us 300mS 200mS 5uS UIC
.FOUR 60Hz 25 I(Einva) V(1020) i(Las)
;.PROBE
.END
```

APPENDIX B
MATLAB® SCRIPT FILES AND OUTPUTS

B.1. The Script for Effective Duty Ratio Calcultaion of Current-Fed Active Filter

<1>. The Harmonic Current Data
File: CI200ULX.m

The harmonic current spectrum:

order	magnitude	phase a (deg.)
1	0.3567	-14.87
5	6.724	-78.64
7	4.55	-97.59
11	2.913	17.77
13	2.461	-9.8
17	1.882	109.4
19	1.682	80.68
23	1.39	-159.2
25	1.278	171.7

<2>. The Main Body Script
File: current.m

```
%Calculate the Duty-Ratios & the Current Required for the Current-fed Inverter
clear;
clc;
%
%Passive filter (60Hz Parallel Resonance)
%Inverter Capacitance := 100uF = Cinv
%
   mx= input('Maximum order of Harmonic (odd)?');
   mo=(mx+1)/2;
   n=1:mo;
   h=2*(n-1)+1;
%
% Get the Information of Current Harmonics
%
```

```
                fid=1;
                load Ci200ULX.m;
                ihm= Ci200ULX(:,2);
                iha_ang= Ci200ULX(:,3)*pi/180;
                fprintf(fid,'\n The harmonic current spectrum: \n');
                fprintf(fid,'\n order     magnitude     phase a (deg.)  \n\n');
for n=1:mo
                if ihm(n) ==0
  else
                fprintf(fid,'%4.0f %13.6g %15.6g \n', h(n), ihm(n), iha_ang(n)*180/pi);
                end
end
%
 dabc_m=zeros(size(ihm));
 da_ang=zeros(size(ihm));
 db_ang=zeros(size(ihm));
 dc_ang=zeros(size(ihm));
                Vcinv=zeros(size(ihm));
                Vcinvm=zeros(size(ihm));
                Vcinv_ang=zeros(size(ihm));
                zf=zeros(size(ihm));
                zhm=zeros(size(ihm));
                zh_ang=zeros(size(ihm));
                iz_eqv=zeros(size(ihm));
                iz_ang=zeros(size(ihm));
%
                wo=2*pi*60;
                Cf=input('Passive Filter Capacitance  (F)? ');
                Lf=input('Passive Filter Inductance   (H)? ');
                Q=input('Quality Factor of the Filter Inductance  ? ');
                R_Lf=wo*Lf/Q;
                R_Cf=R_Lf/10;
                RLdc=0.0;    % Inductor resistce
 Rs=0.1;       % MOSFET on-Resistance, in IGBT Vd
                Von=0.75;    % Diode on-drop
%
                Va_in=input('The 60Hz Source Voltage (Vpeak) ? ');
                iLoad=input('The  60Hz Load Current    (Apeak) ? ');
                iLoad_ang=input('The Phase Angle of Load Current (Deg) ? ');
                Rsa=input('The Power Line Resistance   (ohm) ? ');
                Xsa=input('The Power Line Inductance    (H) ? ');
                Xsa=wo*Xsa;
                Cinv=input('Inverter Capacitance   (F) ? ');
%
for n=1:mo
    zLp=R_Lf+j*h(n)*wo*Lf;
```

```
    zCp=R_Cf-j*1/(h(n)*wo*Cf);
    zf(n)=1/((1/zLp)+(1/zCp));
    zhm(n)=abs(zf(n));
    zh_ang(n)=angle(zf(n));
end
%
                Vdrop=(Rsa+j*Xsa)*iLoad*(cos(iLoad_ang)+j*sin(iLoad_ang));
                Vo=Va_in-Vdrop;
                Vo=Vo/(1+(Rsa+j*Xsa)/zf(1));
                iaf=Vo/zf(1);
%
                ihm(1)=abs(iaf);
                iz_eqv(1)=ihm(1);
                iha_ang(1)=angle(iaf);
                iz_ang(1)=iha_ang(1)+pi;
%
for n=2:mo
                if ihm(n)==0
   else
   kczh= h(n)*wo*Cinv*zhm(n);
                zhih_ang= iha_ang(n)+zh_ang(n)+pi/2;
   kizcomb=2*kczh*(sin(zhih_ang)*sin(iha_ang(n))+cos(zhih_ang)*cos(iha_ang(n)));
   iz_eqv(n)=ihm(n)*sqrt(1+kczh^2+kizcomb);
                 num= kczh*sin(zhih_ang)+sin(iha_ang(n));
                 den= kczh*cos(zhih_ang)+cos(iha_ang(n));
                iz_ang(n)=atan2(num,den)+pi;
   end
end
%
fprintf(fid,'\n The function of [da(t), db(t), dc(t)]*iL contains the following terms: \n');
fprintf(fid,'\n order     magnitude     phase a (deg.)  phase b     phase c\n\n');
ap=iha_ang(1)*180/pi;
ap=phaseangle(ap);
bp= -120+ap;
bp=phaseangle(bp);
cp= 120+ap;
cp=phaseangle(cp);
da_ang(1)=ap;
db_ang(1)=bp;
dc_ang(1)=cp;
fprintf(fid,'%4.0f %13.6g %15.6g %15.6g %15.6g\n', h(1),
iz_eqv(1),da_ang(1),db_ang(1), dc_ang(1));
%
for n=2:mo
    if iz_eqv(n) == 0
        else
```

```
        ap= iz_ang(n)*180/pi;
        ap=phaseangle(ap);
        bp= -120*h(n)+ap;
        bp=phaseangle(bp);
        cp= 120*h(n)+ap;
        cp=phaseangle(cp);
       da_ang(n)=ap;
       db_ang(n)=bp;
       dc_ang(n)=cp;
fprintf(fid,'%4.0f %13.6g %15.6g %15.6g %15.6g\n', h(n), iz_eqv(n),
da_ang(n),db_ang(n), dc_ang(n));
    end
end
%
            i= 0;
            for t=0:0.00005:0.0167
    i=i+1;
    ihx=0;
    i1=iz_eqv(1)*sin(wo*t+iz_ang(1));
    for n=2:mo
       if    ihm(n)==0
       else
       ihx=ihx+iz_eqv(n)*sin(h(n)*wo*t+iz_ang(n));
       end
    itx(i)=ihx+i1;
    end
end
%
            max_I=max(itx);
            min_I=min(itx);
            fprintf(fid,' The maximum of da(t)*iL : %15.6g \n',max_I);
            fprintf(fid,' The minimum of da(t)*iL : %15.6g \n',min_I);
%
            iLneed=1.52*max(abs(itx));
            fprintf(fid,' The inductor current has to set at %12.6g  Adc \n ',iLneed);
%
fprintf(fid,'\n The function of da(t), db(t), dc(t) contains the following terms: \n');
fprintf(fid,'\n order    magnitude    phase a (deg.)   phase b      phase c\n\n');
for n=1:mo
    if iz_eqv(n)== 0
     else
     dabc_m(n)=iz_eqv(n)/iLneed;
     fprintf(fid,'%4.0f %13.6g %15.6g %15.6g %15.6g \n', h(n), dabc_m(n), da_ang(n),
db_ang(n), dc_ang(n));
    end
end
```

```
%
                Vdc=iLneed*(2*Rs+RLdc)+2*Von;
 Pdc=Vdc*iLneed;
                Pac=1.5*abs(Vo)*ihm(1)*cos(angle(Vo)-iha_ang(1));
                fprintf(fid,'\n The DC voltage of the inverter: %10.4g V',Vdc);
                fprintf(fid,'\n The total losses: %10.4g  W \n',Pdc+Pac);
```

<3>. The Script for Transfering Any Angle into [-π, π]
File: phaseangle.m

```
function pp = phaseangle(x)
% Converter any  phase angle within -pi to pi (-180 to 180)
 for n=1:1+abs(round(x))
  if x > 180
    x= x - 360;
  else
     if x < -180
       x= x + 360;
     end
  end
 end
pp= x;
end
```

<4>. The Output List

Maximum order of Harmonic (odd)? 25
The harmonic current spectrum:

order	magnitude	phase a (deg.)
1	0.3567	-14.87
5	6.724	-78.64
7	4.55	-97.59
11	2.913	17.77
13	2.461	-9.8
17	1.882	109.4
19	1.682	80.68
23	1.39	-159.2
25	1.278	171.7

Passive Filter Capacitance (F)? 150e-6
Passive Filter Inductance (H)? 46.91e-3
Quality Factor of the Filter Inductance ? 20
The 60Hz Source Voltage (Vpeak) ? 208
The 60Hz Load Current (Apeak) ? 32.55
The Phase Angle of Load Current (Deg) ? -15,09
The Phase Angle of Load Current (Deg) ? -15.09
The Power Line Resistance (ohm) ? 0.7372
The Power Line Inductance (H) ? 4.572e-3
Inverter Capacitance (F) ? 100e-6

The function of [da(t), db(t), dc(t)]*iL contains the following terms:

order	magnitude	phase a (deg.)	phase b	phase c
1	0.632265	19.3086	-100.691	139.309
5	11.3939	101.981	-138.019	-18.0187
7	7.64722	83.2424	-36.7576	-156.758
11	4.87234	-160.952	-40.9519	79.0481
13	4.1128	171.704	51.7042	-68.2958
17	3.14282	-68.6415	51.3585	171.358
19	2.80846	-97.1339	142.866	22.8661
23	2.32086	23.442	143.442	-96.558
25	2.13402	-5.43004	-125.43	114.57

The maximum of da(t)*iL : 26.9251
The minimum of da(t)*iL : -27.0073
The inductor current has to set at 41.0511 Adc

The function of da(t), db(t), dc(t) contains the following terms:

order	magnitude	phase a (deg.)	phase b	phase c
1	0.0154019	19.3086	-100.691	139.309
5	0.277553	101.981	-138.019	-18.0187
7	0.186285	83.2424	-36.7576	-156.758
11	0.118689	-160.952	-40.9519	79.0481
13	0.100187	171.704	51.7042	-68.2958
17	0.0765588	-68.6415	51.3585	171.358
19	0.0684137	-97.1339	142.866	22.8661
23	0.0565359	23.442	143.442	-96.558
25	0.0519844	-5.43004	-125.43	114.57

The DC voltage of the inverter: 9.71 V
The total losses: 591.5 W

B.2. The Script for Effective Duty Ratio Calcultaion of Voltage-Fed Active Filter

<1>. The Main Body Script
File: volt.m

```
%Calculate the Duty-Ratios & the Voltage Required for the Voltage-fed Inverter
clear;
clc;
%
%Passive filter (60Hz Parallel Resonance)
%Inverter Capacitance := Cinv
%
  mx= input('Maximum order of Harmonic (odd)?');
  mo=(mx+1)/2;
  n=1:mo;
  h=2*(n-1)+1;
%
% Get the Information of Current Harmonics
%
                fid=1;
                load Ci200ULX.m;
                ihm= Ci200ULX(:,2);
                iha_ang= Ci200ULX(:,3)*pi/180;
                fprintf(fid,'\n The harmonic current spectrum: \n');
                fprintf(fid,'\n order     magnitude     phase a (deg.) \n\n');
for n=1:mo
                if ihm(n) ==0
  else
                fprintf(fid,'%4.0f %13.6g %15.6g \n', h(n), ihm(n), iha_ang(n)*180/pi);
                end
end
%
 dabc_m=zeros(size(ihm));
 da_ang=zeros(size(ihm));
 db_ang=zeros(size(ihm));
 dc_ang=zeros(size(ihm));
               Vcinv=zeros(size(ihm));
               Vcinvm=zeros(size(ihm));
               Vcinv_ang=zeros(size(ihm));
               zf=zeros(size(ihm));
               zhm=zeros(size(ihm));
               zh_ang=zeros(size(ihm));
               vz_eqv=zeros(size(ihm));
               vz_ang=zeros(size(ihm));
%
               wo=2*pi*60;
```

```
                Cf=input('Passive Filter Capacitance  (F)? ');
                Lf=input('Passive Filter Inductance   (H)? ');
                Q=input('Quality Factor of the Filter Inductance  ? ');
                R_Lf=wo*Lf/Q;
                R_Cf=R_Lf/10;
                RLdc=0.0;   % Inductor resistce
 Rs=0.1;        % MOSFET on-Resistance, in IGBT Vd
                Von=0.75;   % Diode on-drop
%
                Va_in=input('The 60Hz Source Voltage (Vpeak) ? ');
                iLoad=input('The  60Hz Load Current   (Apeak) ? ');
                iLoad_ang=input('The Phase Angle of Load Current (Deg) ? ');
                Rsa=input('The Power Line Resistance   (ohm) ? ');
                Xsa=input('The Power Line Inductance   (H) ? ');
                Xsa=wo*Xsa;
                Cinv=input('Inverter Capacitance   (F) ? ');
 Linv=input('Inverter Inductance    (H) ?');
%
for n=1:mo
    zLp=R_Lf+j*h(n)*wo*Lf;
    zCp=R_Cf-j*1/(h(n)*wo*Cf);
    zf(n)=1/((1/zLp)+(1/zCp));
    zhm(n)=abs(zf(n));
    zh_ang(n)=angle(zf(n));
end
%
                Vdrop=(Rsa+j*Xsa)*iLoad*(cos(iLoad_ang)+j*sin(iLoad_ang));
                Vo=Va_in-Vdrop;
                Vo=Vo/(1+(Rsa+j*Xsa)/zf(1));
                iaf=Vo/zf(1);
%
                ihm(1)=abs(iaf);
                vz_eqv(1)=ihm(1)*wo*Linv;
                iha_ang(1)=angle(iaf);
                vz_ang(1)=iha_ang(1)+(pi/2)+pi;
%
for n=2:mo
                if ihm(n)==0
   else
   klzh= h(n)*wo*Linv;
   zhih_ang=iha_ang(n)+pi/2;
   kczh=(1-h(n)^2*wo^2*Linv*Cinv)*zhm(n);
   zhvh_ang=iha_ang(n)+zh_ang(n);
   temp1=2*klzh*kczh;
   temp2=sin(zhih_ang)*sin(zhvh_ang)+cos(zhih_ang)*cos(zhvh_ang);
   temp=temp1*temp2;
```

```
   vz_eqv(n)=ihm(n)*sqrt(klzh^2+kczh^2+temp);
   num=klzh*sin(zhih_ang)+kczh*sin(zhvh_ang);
   den=klzh*cos(zhih_ang)+kczh*cos(zhvh_ang);
   vz_ang(n)=atan2(num,den)+pi;
   end
end
%
fprintf(fid,'\n The function of [da(t), db(t), dc(t)]*Vdc contains the following terms: \n');
fprintf(fid,'\n order     magnitude     phase a (deg.)   phase b      phase c\n\n');
ap=vz_ang(1)*180/pi;
ap=phaseangle(ap);
bp= -120+ap;
bp=phaseangle(bp);
cp= 120+ap;
cp=phaseangle(cp);
da_ang(1)=ap;
db_ang(1)=bp;
dc_ang(1)=cp;
fprintf(fid,'%4.0f %13.6g %15.6g %15.6g %15.6g\n', h(1),
vz_eqv(1),da_ang(1),db_ang(1), dc_ang(1));
%
for n=2:mo
    if vz_eqv(n) == 0
       else
         ap= vz_ang(n)*180/pi;
         ap=phaseangle(ap);
         bp= -120*h(n)+ap;
         bp=phaseangle(bp);
         cp= 120*h(n)+ap;
         cp=phaseangle(cp);
       da_ang(n)=ap;
       db_ang(n)=bp;
       dc_ang(n)=cp;
fprintf(fid,'%4.0f %13.6g %15.6g %15.6g %15.6g\n', h(n), vz_eqv(n),
da_ang(n),db_ang(n), dc_ang(n));
    end
end
%
                v= 0;
                for t=0:0.00005:0.0167
    v=v+1;
    vhx=0;
    v1=vz_eqv(1)*sin(wo*t+vz_ang(1));
    for n=2:mo
       if     ihm(n)==0
       else
```

```
        vhx=vhx+vz_eqv(n)*sin(h(n)*wo*t+vz_ang(n));
       end
    vtx(v)=vhx+v1;
    end
end
%
            max_v=max(vtx)*2;
            min_v=min(vtx)*2;
            fprintf(fid,' The maximum of da(t)*Vdc : %15.6g \n',max_v);
            fprintf(fid,' The minimum of da(t)*Vdc : %15.6g \n',min_v);
%
            Vneed=1.02*max(abs(vtx))*2;
            fprintf(fid,' The inductor voltage has to set at %12.6g  Vdc \n ',Vneed);
%
fprintf(fid,'\n The function of da(t), db(t), dc(t) contains the following terms: \n');
fprintf(fid,'\n order     magnitude     phase a (deg.)   phase b      phase c\n\n');
for n=1:mo
   if vz_eqv(n)== 0
    else
    dabc_m(n)=vz_eqv(n)/Vneed;
    fprintf(fid,'%4.0f %13.6g %15.6g %15.6g %15.6g \n', h(n), dabc_m(n), da_ang(n),
db_ang(n), dc_ang(n));
   end
end
%
%
```

<2>. The Output List

Maximum order of Harmonic (odd)?25
The harmonic current spectrum:

order	magnitude	phase a (deg.)
1	0.3567	-14.87
5	6.724	-78.64
7	4.55	-97.59
11	2.913	17.77
13	2.461	-9.8
17	1.882	109.4
19	1.682	80.68
23	1.39	-159.2
25	1.278	171.7

Passive Filter Capacitance (F)? 150e-6

Passive Filter Inductance (H)? 46.91e-3
Quality Factor of the Filter Inductance ? 20
The 60Hz Source Voltage (Vpeak) ? 208
The 60Hz Load Current (Apeak) ? 32.55
The Phase Angle of Load Current (Deg) ? -15.09
The Power Line Resistance (ohm) ? 0.7372
The Power Line Inductance (H) ? 4.572e-3
Inverter Capacitance (F) ? 200e-6
Inverter Inductance (H) ?0.1e-3

The function of [da(t), db(t), dc(t)]*Vdc contains the following terms:

order	magnitude	phase a (deg.)	phase b	phase c
1	0.0238358	-70.6914	169.309	49.3086
5	21.7516	12.964	132.964	-107.036
7	8.90595	-5.25809	-125.258	114.742
11	1.89768	112.968	-127.032	-7.03181
13	0.555666	92.0879	-27.9121	-147.912
17	0.855948	17.3968	137.397	-102.603
19	1.2458	-9.14031	-129.14	110.86
23	1.74562	112.84	-127.16	-7.15997
25	1.90961	84.3423	-35.6577	-155.658

The maximum of da(t)*Vdc : 60.7507
The minimum of da(t)*Vdc : -60.777
The inductor voltage has to set at 61.9925 Vdc

The function of da(t), db(t), dc(t) contains the following terms:

order	magnitude	phase a (deg.)	phase b	phase c
1	0.000384496	-70.6914	169.309	49.3086
5	0.350876	12.964	132.964	-107.036
7	0.143662	-5.25809	-125.258	114.742
11	0.0306114	112.968	-127.032	-7.03181
13	0.00896344	92.0879	-27.9121	-147.912
17	0.0138073	17.3968	137.397	-102.603
19	0.020096	-9.14031	-129.14	110.86
23	0.0281585	112.84	-127.16	-7.15997
25	0.0308038	84.3423	-35.6577	-155.658

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